For all practical purposes, the output characteristics of the common-collector configuration are the same as for the common-emitter configuration. For the common-collector configuration the output characteristics are a plot of $I_E$ versus $V_{EC}$ for a range of values of $I_B$.

The input current, therefore, is the same for both the common-emitter and common collector characteristics. The horizontal voltage axis for the common-collector configuration is obtained by simply changing the sign of the collector-to-emitter voltage of the common-emitter characteristics. Finally, there is an almost unnoticeable change in the vertical scale of $I_C$ of the common-emitter characteristics if $I_C$ is replaced by $I_E$ for the common-collector characteristics (since $\alpha = 1$). For the input circuit of the common-collector configuration the common-emitter base characteristics are sufficient for obtaining the required information.

**LIMITS OF OPERATIONS**

For each transistor there is a region of operation on the characteristics which will ensure that the maximum ratings are not being exceeded and the output signal exhibits minimum distortion. Such a region has been defined for the transistor characteristics of Fig. 3.22. All of the limits of operation are defined on a typical transistor specification sheet described in Section 3.9. Some of the limits of operation are self-explanatory, such as maximum collector current (normally referred to on the specification sheet as continuous collector current) and maximum collector-to-emitter voltage (often abbreviated as $V_{CEO}$ or $V_{BRCEO}$ on the specification sheet). For the transistor of Fig. 3.22, $I_{Cmax}$ was specified as 50 mA and $V_{CEO}$ as 20 V. The vertical line on the characteristics defined as $V_{CEsat}$ specifies the minimum $V_{CE}$ that can be applied without falling into the nonlinear region labeled the saturation region. The level of $V_{CEsat}$ is typically in the neighborhood of the 0.3 V specified for this transistor.
Figure 3.22 Defining the linear (undistorted) region of operation for a transistor.
The maximum dissipation level is defined by the following equation:

\[
P_{C_{\text{max}}} = V_{CE}I_C
\]

For the device of Fig. 3.22, the collector power dissipation was specified as 300 mW. The question then arises of how to plot the collector power dissipation curve specified by the fact that

\[
P_{C_{\text{max}}} = V_{CE}I_C = 300 \text{ mW}
\]

\[
V_{CE}I_C = 300 \text{ mW}
\]

At any point on the characteristics the product of \(V_{CE}\) and \(I_C\) must be equal to 300 mW.

**DC Biasing—BJTs :-**
there is an underlying similarity between the analysis of each configuration due to the recurring use of the following important basic relationships for a transistor:

\[
V_{BE} = 0.7 \text{ V} \quad (4.1)
\]

\[
I_E = (\beta + 1)I_B = I_C \quad (4.2)
\]

\[
I_C = \beta I_B \quad (4.3)
\]

In fact, once the analysis of the first few networks is clearly understood, the path toward the solution of the networks to follow will begin to become quite apparent. In most instances the base current \(I_B\) is the first quantity to be determined. Once \(I_B\) is known, the relationships of Eqs. (4.1) through (4.3) can be applied to find the remaining quantities of interest. The similarities in analysis will be immediately obvious as we progress through the chapter. The equations for \(I_B\) are so similar for a number of configurations that one equation can be derived from another simply by dropping or adding a term or two. The primary function of this chapter is to develop a level of familiarity with the BJT transistor that would permit a dc analysis of any system that might employ the BJT amplifier.

**OPERATING POINT :**
For transistor amplifiers the resulting dc current and voltage establish an operating point on the characteristics that define the region that will be employed for amplification of the applied signal. Since the operating point is a fixed point on the characteristics, it is also called the quiescent point (abbreviated Q-point). By definition, quiescent means quiet, still, inactive. Figure 4.1 shows a general output device characteristic with four operating points indicated. The biasing circuit can be designed to set the device operation at any of these points or others within the active region. The maximum ratings
are indicated on the characteristics of Fig. 4.1 by a horizontal line for the maximum collector current $I_{C\text{max}}$ and a vertical line at the maximum collector-to-emitter voltage $V_{CE\text{max}}$. The maximum power constraint is defined by the curve $P_{C\text{max}}$ in the same figure. At the lower end of the scales are the cutoff region, defined by $I_B \leq 0 \mu A$, and the saturation region, defined by $V_{CE} \leq V_{CE\text{sat}}$. The BJT device could be biased to operate outside these maximum limits, but the result of such operation would be either a considerable shortening of the lifetime of the device or destruction of the device. Confining ourselves to the active region, one can select many different operating areas or points. The chosen Q-point often depends on the intended use of the circuit. For the BJT to be biased in its linear or active operating region the following must be true:

**Linear-region operation:**

1-Base–emitter junction forward biased
2-Base–collector junction reverse biased

Consider first the base–emitter circuit loop of Fig. 4.4. Writing Kirchhoff’s voltage equation in the clockwise direction for the loop, we obtain

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

Note the polarity of the voltage drop across $R_B$ as established by the indicated direction of $I_B$. Solving the equation for the current $I_B$ will result in the following:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

**Figure 4.4 Base–emitter loop.**

**Figure 4.5 Collector–emitter loop.**

The collector–emitter section of the network appears in Fig. 4.5 with the indicated direction of current $I_C$ and the resulting polarity across $R_C$. The magnitude of the collector current is related directly to $I_B$ through

$$I_C = \beta I_B$$
Applying Kirchhoff’s voltage law in the clockwise direction around the indicated closed loop of Fig. 4.5 will result in the following:

\[ V_{CE} + I_C R_C - V_{CC} = 0 \]

\[ V_{CE} = V_{CC} - I_C R_C \]

which states in words that the voltage across the collector–emitter region of a transistor in the fixed-bias configuration is the supply voltage less the drop across \( R_C \). As a brief review of single- and double-subscript notation recall that

\[ V_{CE} = V_C - V_E \]

In addition, since

\[ V_{BE} = V_B - V_E \]

and \( V_E = 0 \) V, then:

\[ V_{BE} = V_B \]

**Example**: Determine the following for the fixed-bias configuration of Fig. 4.7.

(a) \( I_{BQ} \) and \( I_{CQ} \). (b) \( V_{CEQ} \). (c) \( V_B \) and \( V_C \). (d) \( V_{BC} \).

**Solution**

(a) Eq. (4.4): \( I_{BQ} \) = \( \frac{V_{CC} - V_{BE}}{R_B} \) = \( \frac{12 \text{ V} - 0.7 \text{ V}}{240 \text{ k}\Omega} \) = 50.08 mA

(b) Eq. (4.5): \( I_{CQ} \) = \( \beta I_{BQ} \) = (50)(47.08 mA) = 2.35 mA

(c) \( V_B = V_{BE} = 0.7 \) V

\( V_C = V_{CE} = 6.83 \) V

(d) Using double-subscript notation yields

\( V_{BC} = V_B - V_C = 0.7 \text{ V} - 6.83 \text{ V} \)

\( = -6.13 \text{ V} \)

with the negative sign revealing that the junction is reversed-biased, as it should before linear amplification.
Load-Line Analysis:—

The analysis thus far has been performed using a level of $\beta$ corresponding with the resulting Q-point. We will now investigate how the network parameters define the possible range of Q-points and how the actual Q-point is determined. The network establishes an output equation that relates the variables $I_C$ and $V_{CE}$ in the following manner:

$$V_{CE} = V_{CC} - I_C R_C$$

If we choose $I_C$ to be 0 mA, we are specifying the horizontal axis as the line on which one point is located.

$$V_{CE} = V_{CC} - (0)R_C$$

If we now choose $V_{CE}$ to be 0 V, we find that $I_C$ is determined by the following equation:

$$0 = V_{CC} - I_C R_C$$

as appearing on Fig. 4.12.

EXAMPLE:—

Given the load line of Fig. 4.16 and the defined Q-point, determine the required values of $V_{CC}$, $R_C$, and $R_B$ for a fixed-bias configuration.

Solution

From Fig. 4.16,

$$V_{CE} = V_{CC} = 20 \text{ V} \text{ at } I_C = 0 \text{ mA}$$

$$I_C = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0 \text{ V}$$

$$R_C = \frac{V_{CC}}{I_C} = \frac{20 \text{ V}}{10 \text{ mA}} = 2 \text{ k}\Omega$$
EMITTER-STABILIZED BIAS CIRCUIT:

The dc bias network of Fig. 4.17 contains an emitter resistor to improve the stability level over that of the fixed-bias configuration. The improved stability will be demonstrated through a numerical example later in the section. The analysis will be performed by first examining the base–emitter loop and then using the results to investigate the collector–emitter loop.

The base–emitter loop of the network of Fig. 4.17 can be redrawn as shown in Fig. 4.18. Writing Kirchhoff’s voltage law around the indicated loop in the clockwise direction will result in the following equation:

\[ +V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0 \]

\[ I_E = (\beta + 1)I_B \]

Substituting for \( I_E \) in Eq. will result in

\[ V_{CC} - I_B R_B - V_{BE} - (\beta + 1)I_E R_E = 0 \]

\[ I_E(P_B + (\beta + 1)R_E) + V_{CC} + V_{BE} = 0 \]

\[ I_E(P_B + (\beta + 1)R_E) = V_{CC} - V_{BE} \]

and solving for \( I_B \) gives

\[ I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} \]
The collector–emitter loop is redrawn in Fig. 4.21. Writing Kirchhoff’s voltage law for the indicated loop in the clockwise direction will result in:

\[ +I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0 \]

Substituting \( I_E = I_C \) and grouping terms gives:

\[ V_{CE} - V_{CC} + I_C (R_C + R_E) = 0 \]

\[ V_{CE} = V_{CC} - I_C (R_C + R_E) \]

The single-subscript voltage \( V_E \) is the voltage from emitter to ground and is determined by:

\[ V_E = I_E R_E \]

while the voltage from collector to ground can be determined from:

\[ V_{CE} = V_C - V_E \]

\[ V_C = V_{CE} + V_E \]

\[ V_C = V_{CC} - I_C R_C \]

The voltage at the base with respect to ground can be determined from:

\[ V_B = V_{CC} - I_B R_B \]

\[ V_B = V_{BE} + V_E \]

**EXAMPLE:** For the emitter bias network of Fig. 4.22, determine:

(a) \( I_B \). (b) \( I_C \). (c) \( V_{CE} \). (d) \( V_C \). (e) \( V_E \). (f) \( V_B \). (g) \( V_{BC} \).

\[ I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E} = \frac{20 \, \text{V} - 0.7 \, \text{V}}{430 \, \text{k}\Omega + (51)(1 \, \text{k}\Omega)} \]

\[ = \frac{19.3 \, \text{V}}{481 \, \text{k}\Omega} = 40.1 \, \mu\text{A} \]

(b) \( I_C = \beta I_B \)

\[ = (50)(40.1 \, \mu\text{A}) \]

\[ = 2.01 \, \text{mA} \]

\[ V_{CE} = V_{CC} - I_C (R_C + R_E) \]

\[ = 20 \, \text{V} - (2.01 \, \text{mA})(2 \, \text{k}\Omega + 1 \, \text{k}\Omega) \]

\[ = 13.97 \, \text{V} \]

(d) \( V_C = V_{CC} - I_C R_C \)

\[ = 20 \, \text{V} - (2.01 \, \text{mA})(2 \, \text{k}\Omega) \]
\( V_E = V_C - V_{CE} \)
\[ = 15.98 \text{ V} - 13.97 \text{ V} \]
\[ = 2.01 \text{ V} \]

or

\( V_E = I_E R_E = I_C R_E \)
\[ = (2.01 \text{ mA})(1 \text{ k}\Omega) \]
\[ = 2.01 \text{ V} \]

\( V_B = V_{BE} + V_E \)
\[ = 0.7 \text{ V} + 2.01 \text{ V} \]
\[ = 2.71 \text{ V} \]

\( V_{BC} = V_B - V_C \)
\[ = 2.71 \text{ V} - 15.98 \text{ V} \]
\[ = -13.27 \text{ V} \) (reverse-biased as required)

**VOLTAGE-DIVIDER BIAS:**

In the previous bias configurations the bias current \( I_{CQ} \) and voltage \( V_{CEQ} \) were a function of the current gain (\( \beta \)) of the transistor. However, since \( \beta \) is temperature sensitive, especially for silicon transistors, and the actual value of beta is usually not well defined, it would be desirable to develop a bias circuit that is less dependent, or in fact, independent of the transistor beta. The voltage-divider bias configuration of Fig. 4.25 is such a network. If analyzed on an exact basis the sensitivity to changes in beta is quite small. If the circuit parameters are properly chosen, the resulting levels of \( I_{CQ} \) and \( V_{CEQ} \) can be almost totally independent of beta. Recall from previous discussions that a Q-point is defined by a fixed level of \( I_{CQ} \) and \( V_{CEQ} \). The level of \( I_{BQ} \) will change with the change in beta, but the operating point on the characteristics defined by \( I_{CQ} \) and \( V_{CEQ} \) can remain fixed if the proper circuit parameters are employed. As noted above, there are two methods that can be applied to analyze the voltage divider configuration.

![Figure 4.25](image1.png)  
*Figure 4.25* Voltage-divider bias

![Figure 4.27](image2.png)  
*Figure 4.27* Redrawing the input side of the network of Fig. 4.25.
1- Exact Analysis :

\[ R_{Th} = R_1 || R_2 \]

The voltage source is replaced by a short-circuit equivalent.

**ETh:** The voltage source \( V_{CC} \) is returned to the network and the open-circuit Thévenin voltage determined as follows: Applying the voltage-divider rule:

\[ E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2} \]

The Thévenin network is then redrawn, and \( I_E \) can be determined by first applying Kirchhoff’s voltage law in the clockwise direction for the loop indicated:

\[ E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0 \]

Substituting \( I_E = (\beta + 1)I_B \) and solving for \( I_B \) yields

\[ I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} \]

Once \( I_B \) is known, the remaining quantities of the network can be found in the same manner as developed for the emitter-bias configuration. That is,

\[ V_{CE} = V_{CC} - I_C (R_C + R_E) \]

2- Approximate Analysis :

The input section of the voltage-divider configuration can be represented by the network of Fig. 4.32. The resistance \( R_i \) is the equivalent resistance between base and ground for the transistor with an emitter resistor \( R_E \) that the reflected resistance between base and emitter is defined by \( R_i (\beta + 1)R_E \). If \( R_i \) is much larger than the resistance \( R_2 \), the current \( I_B \) will be much smaller than \( I_2 \) (current always seeks the path of least resistance) and \( I_2 \) will be approximately equal to \( I_1 \). If we accept the approximation that \( I_B \) is essentially zero amperes compared to \( I_1 \) or \( I_2 \), then \( I_1 = I_2 \) and \( R_1 \) and \( R_2 \) can be considered series ele-

---

**Figure 4.32** Partial-bias circuit for calculating the approximate base voltage \( V_B \).
ments. The voltage across $R_2$, which is actually the base voltage, can be determined using the voltage-divider rule (hence the name for the configuration). That is,

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Since $Ri = (\beta+1)R_E = \beta R_E$, the condition that will define whether the approximate approach can be applied will be the following:

$$\beta R_E \geq 10R_2$$

In other words, if $\beta$ times the value of $R_E$ is at least 10 times the value of $R_2$, the approximate approach can be applied with a high degree of accuracy. Once $V_B$ is determined, the level of $V_E$ can be calculated from

$$V_E = V_B - V_{BE}$$

and the emitter current can be determined from:

$$I_E = \frac{V_E}{R_E}$$

$$I_{CQ} \approx I_E$$

The collector-to-emitter voltage is determined by:

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$V_{CEQ} = V_{CC} - I_C (R_C + R_E)$$

The Q-point (as determined by $I_{CQ}$ and $V_{CEQ}$) is therefore independent of the value of $\beta$.

**DC BIAS WITH VOLTAGE FEEDBACK**:

An improved level of stability can also be obtained by introducing a feedback path from collector to base as shown in Fig. 4.34. Although the Q-point is not totally independent of beta (even under approximate conditions), the sensitivity to changes in beta or temperature variations is normally less than encountered for the fixed-bias or emitter-biased configurations. The analysis will again be performed by first analyzing the base–emitter loop with the results applied to the collector–emitter loop.

**Base–Emitter Loop**:

Figure 4.35 shows the base–emitter loop for the voltage feedback configuration. Writing Kirchhoff’s voltage law around the indicated loop in the clockwise direction will result in

$$V_{CC} - I_C R_C - I_B R_B - V_{BE} - I_E R_E = 0$$
It is important to note that the current through $R_C$ is not $I_C$ but $I_C' = I_C + I_B$. However, the level of $I_C$ and $I_C'$ far exceeds the usual level of $I_B$ and the approximation $I_C' \approx I_C$ is normally employed. Substituting $I_C' \approx I_C = \beta I_B$ and $I_E \approx I_C$ will result in

$$ V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0 $$

Gathering terms, we have:

$$ V_{CC} - V_{BE} - \beta I_B (R_C + R_E) - I_B R_B = 0 $$

and solving for $I_B$ yields:

$$ I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta (R_C + R_E)} $$

The result is quite interesting in that the format is very similar to equations for $I_B$ obtained for earlier configurations. The numerator is again the difference of available voltage levels, while the denominator is the base resistance plus the collector and emitter resistors reflected by $\beta$. In general, therefore, the feedback path results in a reflection of the resistance $R_C$ back to the input circuit, much like the reflection of $R_E$. In general, the equation for $I_B$ has had the following format:

$$ I_B = \frac{V'}{R_B + \beta R'} $$

with the absence of $R'$ for the fixed-bias configuration, $R' = R_E$ for the emitter-bias setup (with $(\beta + 1) \equiv \beta$), and $R' = R_C + R_E$ for the collector-feedback arrangement. The voltage $V'$ is the difference between two voltage levels.

Since $I_C = \beta I_B$, in general, the larger $\beta R'$ is compared to $R_B$, the less the sensitivity of $I_{C_0}$ to variations in $\beta$. Obviously, if $\beta R' \gg R_B$ and $R_B + \beta R' \equiv \beta R'$, then

$$ I_{C_0} = \frac{\beta V'}{R_B + \beta R'} \approx \frac{\beta V'}{\beta R'} = \frac{V'}{R'} $$

and $I_{C_0}$ is independent of the value of $\beta$. Since $R'$ is typically feedback configuration than for the emitter-bias configuration, variations in $\beta$ is less. Of course, $R'$ is zero ohms for the fixed-bias, therefore quite sensitive to variations in $\beta$.

**Collector–Emitter Loop:**

The collector–emitter loop for the network is provided in Fig. 4.36. Applying Kirchhoff’s voltage law around the indicated loop in the clockwise direction will result in

$$ V_{CE} = I_E R_E $$
The circuit input will be connected to the base of a transistor, and the emitter is connected to the output, while the collector will be joint to the common (earth). This circuit used for matching between circuits cause it has high input impedance and low output impedance. We can get more knowledge about it from these examples.

**EXAMPLE:-** Determine $V_{CEO}$ and $I_E$ for the network.

Applying Kirchhoff’s voltage law to the input circuit will result in:

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

$$I_E = (\beta + 1)I_B$$

$$V_{EE} - V_{BE} - (\beta + 1)I_B R_E - I_B R_B = 0$$

$$I_B = \frac{V_{EE} - V_{BE}}{R_E + (\beta + 1)R_E}$$

Substituting values yields:

$$I_B = \frac{20 \text{ V} - 0.7 \text{ V}}{240 \text{ kΩ} + (91)(2 \text{ kΩ})}$$

$$= \frac{19.3 \text{ V}}{240 \text{ kΩ} + 182 \text{ kΩ}} = \frac{19.3 \text{ V}}{422 \text{ kΩ}}$$

$$= 45.73 \text{ μA}$$

$$I_C = \beta I_B$$

$$= (90)(45.73 \text{ μA})$$

$$= 4.12 \text{ mA}$$

Applying Kirchhoff’s voltage law to the output circuit, we have:

$$-V_{EE} + I_E R_E + V_{CE} = 0$$

$$I_E = (\beta + 1)I_B$$

$$V_{CEQ} = V_{EE} - (\beta + 1)I_B R_E$$

$$= 20 \text{ V} - (91)(45.73 \text{ μA})(2 \text{ kΩ})$$

$$= 11.68 \text{ V}$$

$$I_E = 4.16 \text{ mA}$$
Common-base Amplifier:
The circuit input will be connected to emitter of a transistor, and the collector is connected to the output, while the base will be joint to the common (earth). This circuit used for voltage amplification cause it has low input impedance and high output impedance. We can get more knowledge about it from these examples.

EXAMPLE: Determine the voltage $V_{CB}$ and the current $I_B$ for the common-base configuration?

Solution:
Applying Kirchhoff’s voltage law to the input circuit yields

$$-V_{EE} + I_E R_E + V_{BE} = 0$$

$$I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

Substituting values, we obtain

$$I_E = \frac{4 \, \text{V} - 0.7 \, \text{V}}{1.2 \, \text{k}\Omega} = 2.75 \, \text{mA}$$

Applying Kirchhoff’s voltage law to the output circuit gives:

$$-V_{CB} + I_c R_C - V_{CC} = 0$$

$$V_{CB} = V_{CC} - I_c R_C \text{ with } I_c = I_E$$

$$= 10 \, \text{V} - (2.75 \, \text{mA})(2.4 \, \text{k}\Omega)$$

$$= 3.4 \, \text{V}$$

$$I_B = \frac{I_C}{\beta}$$

$$= \frac{2.75 \, \text{mA}}{60}$$

$$= 45.8 \, \mu\text{A}$$
The AC Load Line:
For a system such as appearing in Fig. 10.9a, the dc load line was drawn on the output characteristics as shown in Fig. 10.9b. The load resistance did not contribute to the dc load line since it was isolated from the biasing network by the coupling capacitor ($C_C$). For the ac analysis, the coupling capacitors are replaced by a short-circuit equivalence that will place the load and collector resistors in a parallel arrangement defined by:

$$R'_L = R_C \parallel R_L$$

The effect on the load line is shown in Fig. 10.9b with the levels to determine the new axes intersections. Note of particular importance that the ac and dc load lines pass through the same Q-point—a condition that must be satisfied to ensure a common solution for the network under dc and/or ac conditions.

For the unloaded situation, the application of a relatively small sinusoidal signal to the base of the transistor could cause the base current to swing from a level of $I_{B2}$ to $I_{B4}$ as shown in Fig. 10.9b. The resulting output voltage $v_{ce}$ would then have the swing appearing in the same figure. The application of the same signal for a loaded situation would result in the same swing in the $I_{B}$ level, as shown in Fig. 10.9b. The result, however, of the steeper slope of the ac load line is a smaller output voltage.

Example:
The figure show an amplifier stage with linear char. as shown in table below. The coupling impedance of capacitors is negligible. $v_i = 0.5 \sin wt$, $R_s=10K\Omega$ , $R_i=2.5K\Omega$ . Calculate $A_i$, $A_v$, $A_p$?

<table>
<thead>
<tr>
<th>$I_B$ (μA)</th>
<th>0</th>
<th>20</th>
<th>40</th>
<th>60</th>
<th>80</th>
<th>100</th>
<th>120</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CE}(V)$</td>
<td>1</td>
<td>10</td>
<td>1</td>
<td>10</td>
<td>1</td>
<td>10</td>
<td>1</td>
</tr>
<tr>
<td>$I_C$ (mA)</td>
<td>0.2</td>
<td>0.2</td>
<td>0.88</td>
<td>1.4</td>
<td>1.7</td>
<td>2.38</td>
<td>2.69</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>$A_i$</th>
<th>$A_v$</th>
<th>$A_p$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
For DC load line:
\[ V_{CEm} = V_{CC} \text{ at } I_C = 0 \text{ mA} \]
\[ V_{CEm} = 12 \text{ V} \]
\[ I_{Cm} = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0 \text{ V} \]
\[ I_{Cm} = 12 / 2 = 6 \text{ mA} \]
\[ I_{BO} = \frac{V_{CC} - V_{BE}}{R_B} = 12 - 0.7 / 188 \times 10^3 = 60 \mu A \]
\[ i_B = \frac{V_S}{R_S + R_i} = 0.5 / 10 + 2.5 = 40 \mu A \]
\[ i_B = 40 \text{ Sin wt} \]
\[ \text{Base current varies between:} \]
\[ 60 + 40 = 100 \mu A \]
\[ 60 - 40 = 20 \mu A \]
\[ \Delta i_B = 100 - 20 = 80 \mu A \]
From the plotted figure (output char.):
\[ I_{CQ} = 3 \text{ mA} , \ V_{CEQ} = 6 \text{ V} \]
\[ I_C = I_{CQ} + V_{CEQ} / R_P = 3 + 6 / 1 = 9 \text{ mA} \]
\[ V_{CE} = V_{CEQ} + I_{CQ} \times R_P = 6 + 3 \times 1 = 9 \text{ V} \]
\[ \Delta i_C = 4.9 - 1.2 = 3.7 \text{ mA} \]
\[ \Delta i_C / \Delta i_B = 3.7 \times 10^3 / 80 = 46 \text{ times} \]
\[ \Delta i (\text{stage}) = \Delta i \times RC / RC + RL = 46 \times 2 / 4 = 23 \text{ times} \]
\[ \Delta v_{CE} = 7.9 - 4.1 = 3.8 \text{ V} \]
\[ \Delta v_i = \Delta i_B \times R_i = 80 \times 10^{-6} \times 2.5 \times 10^3 = 0.2 \text{ V} \]
\[ \Delta v = \Delta v_{CE} / \Delta v_i = 3.8 / 0.2 = 19 \text{ times} \]

\[ A_P = A_i \times A_v = 23 \times 19 = 437 \text{ times} \]

TRANSISTOR SWITCHING NETWORKS:

The application of transistors is not limited solely to the amplification of signals. Through proper design it can be used as a switch for computer and control applications. The network of Fig. 4.52 can be employed as an inverter in computer logic circuitry. Note that the output voltage \( V_C \) is opposite to that applied to the base or input terminal. In addition, note the absence of a dc supply connected to the base circuit.

The only dc source is connected to the collector or output side and for computer applications is typically equal to the magnitude of the “high” side of the applied signal, in this case 5 V.

Proper design for the inversion process requires that the operating point switch from cutoff to saturation along the load line. For our purposes we will assume that \( I_C = I_{CEO} = 0 \) mA when \( I_B = 0 \) \( \mu \)A (an excellent approximation in light of improving construction techniques). In addition, we will assume that \( V_{CE} = V_{CE_{sat}} = 0 \) V rather than the typical 0.1- to 0.3-V level. When \( V_i = 5V \), the transistor will be “on” and the design must ensure that the network is heavily saturated by a level of \( I_B \) greater than that associated with the \( I_B \) curve appearing near the saturation level. this requires that \( I_B > 50 \) \( \mu \)A. The saturation level for the collector current for the circuit of Fig. 4.52 is defined by:

\[
I_{C_{sat}} = \frac{V_{CC}}{R_C}
\]

The level of \( IB \) in the active region just before saturation results can be approximated by the following equation:

\[
I_{B_{max}} = \frac{I_{C_{sat}}}{\beta_{dc}}
\]

For the saturation level we must therefore ensure that the following condition is satisfied:

\[
I_B > \frac{I_{C_{sat}}}{\beta_{dc}}
\]
when \( V_i = 5 \) V, the resulting level of \( I_B \) is the following:

\[
I_B = \frac{V_i - 0.7 \text{ V}}{R_B} = \frac{5 \text{ V} - 0.7 \text{ V}}{68 \text{ k}\Omega} = 63 \mu\text{A}
\]

\[
I_{C_{\text{sat}}} = \frac{V_{CC}}{R_C} = \frac{5 \text{ V}}{0.82 \text{ k}\Omega} \equiv 6.1 \text{ mA}
\]

\[
I_B = 63 \mu\text{A} > \frac{I_{C_{\text{sat}}}}{\beta_{\text{dc}}} = \frac{6.1 \text{ mA}}{125} = 48.8 \mu\text{A}
\]

which is satisfied. Certainly, any level of \( I_B \) greater than 60 \( \mu \)A will pass through a Q-point on the load line that is very close to the vertical axis.

For \( V_i = 0 \) V, \( I_B = 0 \) \( \mu \)A, and since we are assuming that \( I_C = I_{CEO} = 0 \) mA, the voltage drop across \( RC \) as determined by \( V_{RC} = I_C R_C = 0 \) V, resulting in \( V_C = +5 \) V for the response indicated in Fig. 4.52.

In addition to its contribution to computer logic, the transistor can also be employed as a switch using the same extremities of the load line. At saturation, the current \( I_C \) is quite high and the voltage \( V_{CE} \) very low. The result is a resistance level between the two terminals determined by:

\[
R_{\text{sat}} = \frac{V_{CE_{\text{sat}}}}{I_{C_{\text{sat}}}}
\]

Using a typical average value of \( V_{CE_{\text{sat}}} \) such as 0.15 V gives:

\[
R_{\text{sat}} = \frac{0.15 \text{ V}}{6.1 \text{ mA}} = 24.6 \Omega
\]

which is a relatively low value and =0 when placed in series with resistors in the kilohm range. For \( V_i = 0 \) V, the cutoff condition will result in a resistance level of the following magnitude:

\[
R_{\text{cutoff}} = \frac{V_{CC}}{I_{CEO}} = \frac{5 \text{ V}}{0 \text{ mA}} = \infty \Omega
\]

resulting in the open-circuit equivalence. For a typical value of \( I_{CEO} = 10 \mu\text{A} \), the magnitude of the cutoff resistance is:

\[
R_{\text{cutoff}} = \frac{V_{CC}}{I_{CEO}} = \frac{5 \text{ V}}{10 \mu\text{A}} = 500 \text{ k}\Omega
\]

which certainly approaches an open-circuit equivalence for many situations.