Q1: Define **Five** of the following:
Distributed computing, MPC, RL, Z and Y registers, MAR, Pipelining.  

(10 marks)

Q2: Give **one** reason for the following (choose 5):  
1- Use SAFE POP routine for STACK operations.
2- Use TTY (in, out) BUFFERS between CPU & I/O Devises.
3- Use Step Decoder in CU.
4- Use LINK MEMORY LOCATION.
5- CPU using to the PSW.
6- Gourd Bit existing in floating point numbers.

(10 marks)

Q3: Answer **two** of the following:  
1- Draw the Organization of the Control Unit to enable conditional branching in the Micro Programming.
2- Draw how CPU ask the main memory (main store) the data and write it in the cache.
3- Computer Organization.

(10 marks)

Q4: Write the control sequence to execute instruction "ADD" the contents of M.L. whose address in R2 and M.L. whose address is result from adding PC update value and MDR value), store the result in R3.  

(10 marks)

Q5: Solve the following:  
1- Multiply 2 by 16 (ALU Multiplication method).
2- BIC B # 253, # 172.

(10 marks)

Q6: Depending on your specification explain with example the Cache memory size effect on:
1- Artificial hand designing (AI Specification).
2- Camera security system in the banks (Computer Security Specification).
3- chronic disease patients database creation for all hospitals in Iraq (Information System Specification).
4- Iris image processing in the airports (Software specification).  

(20 marks)

GOOD LUCK