Q1-1 (12marks) The PC based system shown in Fig. Q1-1 is used to activate a 220v a.c. cooling system if the temperature T increases above 30°C and turn the system off if the temperature decreases below 20°C.

A- (7marks) Interface the system to the computer using the ISA bus. Use address 300H for start conversion and to read converted data. Use the address 301H for checking end of conversion. Use the address 302H to set or reset the JK FF.

B- (4marks) Write instructions to read a sample of T and store it (in its digital form) in memory location TM. C- (1mark) What is the minimum change in temperature that could be sensed by the A/D converter?

---

**Answer either Q1-1 or Q1-2**

A- (7marks) Interface the system to the computer using the ISA bus. Use address 300H for start conversion and to read converted data. Use the address 301H for checking end of conversion. Use the address 302H to set or reset the JK FF.

B- (4marks) Write instructions to read a sample of T and store it (in its digital form) in memory location TM. C- (1mark) What is the minimum change in temperature that could be sensed by the A/D converter?

---

**Answer C here**

\[
\frac{50}{255} \degree C
\]
Q1-2 (12 marks) The PC based system shown in Fig. Q1-2 is used to activate a 220v a.c. cooling system if the temperature \( T \) increases above 30°C and turn the system off if the temperature decreases below 20°C.

A- (7 marks) Interface the system to the computer using the ISA bus. Use addresses between 3F9H and 3FFH. Use the given A/D as 8 bit A/D.

B- (4 marks) Write instructions to read a sample of \( T \) and store it (in its digital form) in memory location \( TM \). C- (1 mark) What is the minimum change in temperature that could be sensed by the A/D converter?

Answer B here

| OUT 3FDH, x | Initiate 8bit Conv. |
| A=1N 3FFH | check conv. status |
| A= A and 1 | 
| IF A=1 Then X | 
| TM= INP 3FCH | Read T (in dig. form) |

Answer C here

\[
\frac{80}{255} \]

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Q2 (3 marks) If the noise source in Figure 2 has an amplitude of 30 Volts, then what will be the noise voltage seen across the receiver at \( V_0 \)?

\[
V_n \text{ at } V_0 = \frac{30V}{(10 + 250 + 3 \times 10) \Omega} = 0.0025 \text{ V}
\]

Figure Q2

Q3 (5 marks) Figure Q3a shows the waveforms for a 2-channel optical incremental encoder intended to measure an angular movement with the help of a counter IC.

![Waveforms](image)

**Figure Q3a**

Complete the design of the cct in Figure Q3b so that the cct can detect rotation as well as rotation direction and produces two signals, one signal to declare CW rotation (to make the counter counts up) or to declare CCW rotation (to make the counter counts down). And the other signal is for producing counting pulses, i.e., clock signal.

![Circuit Diagram](image)

**Figure Q3b**
Q4 (22 marks (15+7))

A- (15marks) Interface (simultaneously) the ICs of Figure Q4 to the parallel port. Notice that part of the design is given and it is required to complete the uncompleted part. Use a decoding circuit in your design which depends on Table 1 (Note: Table 1 is uncompleted and you should complete it first).

<table>
<thead>
<tr>
<th>Decoding circuit inputs</th>
<th>Signals to be fed by the decoding circuit outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>OE (ADC 0808)</td>
</tr>
<tr>
<td>C3 Prt</td>
<td>C1 Prt</td>
</tr>
<tr>
<td>--------</td>
<td>--------</td>
</tr>
<tr>
<td>0 0 0</td>
<td>1 0 1 1 1 1 0</td>
</tr>
<tr>
<td>0 0 1</td>
<td>0 1 1 1 1 1 0</td>
</tr>
<tr>
<td>0 1 1</td>
<td>0 0</td>
</tr>
<tr>
<td>0 1 0</td>
<td>0 0</td>
</tr>
<tr>
<td>0 0 0</td>
<td>0 0</td>
</tr>
<tr>
<td>0 1 0</td>
<td>0 0</td>
</tr>
<tr>
<td>0 1 1</td>
<td>0 0</td>
</tr>
<tr>
<td>0 1 1</td>
<td>0 0</td>
</tr>
</tbody>
</table>

OE(808) = C3 + C1 + C0  
SC/ALE(808) = C3 + C1 + C0  
WR(7226) = C3 + C1 + C0  
WR(8255) = C3 + C1 + C0  
RD(8255) = C3 + C1 + C0  
C3(8255) = (C3 + C1 + C0) - (C3 + C1 + C0)  
E(Latch) = C3 + C1 + C0
(7 Marks) Write a program which just does the following two steps:
- Order the ADC0808 to select channel IN0 and start conversion.
- Send the value in a memory location M1 to the AD7226.

The base address for the parallel port is 378H.

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Comment</th>
<th>C7</th>
<th>C6</th>
<th>C5</th>
<th>C4</th>
<th>C3</th>
<th>C2</th>
<th>C1</th>
<th>C0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Out 37AH, 0</td>
<td>Internally input port: Set D.C. for OIP externally: Do nothing state.</td>
<td></td>
<td></td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Out 37AH, 10</td>
<td>Activate SC1ALE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Out 378H, 0</td>
<td>Choose channel IN0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Out 37AH, 0</td>
<td>Start conversion</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Go to do nothing state</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Out 37AH, 2</td>
<td>Set DG for OIP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Enable latch</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Out 378H, 0</td>
<td>Choose OUT A in 7226</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Out 37AH, 0</td>
<td>Disable latch</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Go to do nothing</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Out 378H, M1</td>
<td>Output data of M1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Out 37AH, 9</td>
<td>Activate WR (7226) to receive M1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Out 37AH, 0</td>
<td>De-activate WR (7226)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Go to do nothing</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**Q5 (30 marks):** Figure Q5a represents a block diagram for the position control system of figure Q5b. It is desired to use a digital computer to replace the components which its function could be implemented as software by the computer. The new block diagram for the new system when the computer is used is given in Figure Q5c.

![Figure Q5a](image)

![Figure Q5b](image)

![Figure Q5c](image)

(MC: Modification Cct) (DA: Dig. to An. Converter) (AD: An. to Dig. Converter) (FA and FD are conversion functions)

**Figure Q5c**
**A- (10 marks):** Find the equations for IP, ED, At1, At2, PA, FA1, FA2, FD1, FD2.

<table>
<thead>
<tr>
<th>IP</th>
<th>[ V_i = \frac{12V}{90^\circ} ]</th>
</tr>
</thead>
<tbody>
<tr>
<td>ED</td>
<td>[ E = -\left( R_1 \frac{V_i}{R_3} + R_2 \frac{V_{fa}}{R_{fa}} \right) ]</td>
</tr>
</tbody>
</table>

| At1 | \[ V_i = \frac{R_i}{R} E \Rightarrow V_i = 0.5E \] |
| At2 | \[ V_2 = \frac{V_i^2}{R} \Rightarrow V_i = 0.5 \frac{V_i}{R} \] |

| PA | \[ V_{o1a} = 12V \] for \( (V_i - V_2) > 12V \) |
|    | \[ V_{o1a} = \frac{12}{12} (V_i - V_2) \] for \( 0 \leq V_i - V_2 \leq 12 \) |
|    | \[ V_{o1a} = 0V \] for \( V_i - V_2 < 0V \) |

| FA1 | \[ V_{fa} = \frac{255}{2V} \] |
| FA2 | \[ S_a = \left( S_d - \frac{255}{2} \right) \frac{2V_a}{255} \] |

| FD1 | \[ V_{o1a} = \frac{12V}{255} V_{o1d} \] |
| FD2 | \[ V_{o2a} = \frac{12V}{255} V_{o2d} \] |
B- (10 marks) Depending on Figure Q5c Interface the system to the computer using the ISA bus and using the following ICs: ADC0808 (A to D which gives 0H for 0V and FFH for 5V), AD7226 (D to A which gives 0V for 0H and 12V for FFH). For the A/D use addresses 304H and 305H. For the D/A use addresses 300H to 303H.

\[ V_{o1}' = V_{o1} \]

\[ V_{o2}' = V_{o2} \]

note: no need for MC3 & MC4

\[ Out = \frac{5}{24} In + \frac{5}{2} \]

I/O Relationship for MC1 & MC2
**C- (10 marks)** Write a program which does the following steps:
- Deciding \( \theta_i \) value (considering it a step input), and find \( V_i \)
- Read a sample of \( S \) and a sample of \( V_f \), i.e. get \( S_d \) and \( V_f_d \).
- Find \( V_f a \) - Find \( E \) - Find \( V_1 \) - Find \( S_a \) - Find \( V_2 \)
- Find \( V_{o1a} \) - Find \( V_{o2a} \) - Find \( V_{o1d} \) - Find \( V_{o2d} \)
- Send each of \( V_{o1d} \) and \( V_{o2d} \) to the D/A.

<table>
<thead>
<tr>
<th>Instructions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Give ( \theta_i )</td>
</tr>
<tr>
<td>( V_i = \frac{12}{\theta_i} )</td>
</tr>
<tr>
<td>out 304H,1</td>
</tr>
</tbody>
</table>

\[ E_{oc} = INP 305H \]  
get \( S_d \)  
IF \( E_{oc} = 0 \) then \(*\)  
\( S_d = INP 304H \)  
out 304H,0  
\[ E_{oc} = INP 305H \]  
get \( V_{o1h} \)  
IF \( E_{oc} = 0 \) then \(*\)  
\( V_{pd} = INP 304H \)  
\( V_{pa} = \frac{24}{255} (V_{pd} - \frac{255}{2}) \)  
\( E = - (V_i + V_{pa}) \)  
\( V_i = 0.5 E \)  
\( S_a = (S_d - \frac{255}{2}) \frac{24}{255} \)  
\( V_2 = 0.5 S_a \)  
if \( V_1 - V_2 \geq 12 \) then \( V_{o1a} = 12 \)  
if \( 0 \leq V_1 - V_2 \leq 12 \) then \( V_{o1a} = V_1 - V_2 \)  
if \( V_1 - V_2 < 0 \) then \( V_{o1a} = 0 \)  
if \( V_1 - V_2 \leq -12 \) then \( V_{o2a} = 12 \)  
if \( -12 \leq V_1 - V_2 \leq 0 \) then \( V_{o2a} = V_2 - V_1 \)  
if \( V_1 - V_2 > 0 \) then \( V_{o2a} = 0 \)  
\( V_{o1d} = INT (\frac{255}{12} ) V_{o1a} \)  
\( V_{o2d} = INT (\frac{255}{12} ) V_{o2a} \)  
out 300H, V_{o1d}  
out 301H, V_{o2d}
Q6-1 (10 marks) Figure Q6-1a represents a block diagram for the level control system of figure Q6-1b. It is desired to use a digital computer to replace any part which its function could be implemented as software by the computer. On figure Q6-1a, mark with (__) the parts that could be replaced. Then design the hardware part to connect the remainder of the system to the computer using the ISA bus and the following ICs: AD0804(A/D), and 74374 latch. Use addresses between 300H and 303H and as needed.

In your design, consider or suppose the followings:
N1 and N2 are logic signals that takes the value 0V (logic 0) or 5V (logic 1). And, the signal Pv is an analog voltage between 0V and 5V. The AD0804 accepts 0-5V at its analog in.

Figure 6-1a

Figure 6-1b
Q6-2 (10 marks) Figure Q6-2 represents a block diagram for a speed control system. It is desired to use a digital computer to replace any part which its function could be implemented as software by the computer. On figure Q6-2 mark with ( ) the parts that could be replaced. Then, design the hardware part to connect the remainder of the system to the computer using the ISA bus and the following ICs: AD574 (use it as an 8 bits A/D), and AD7226 (D/A). Use addresses between 300H and 30FH and as needed.

Consider that the AD574 is to be connected to give 0 for -10V and FFH for +10V, and the AD7226 gives 0V for 0 and 12V for FFH. For the Pre Amp I/O relations, refer to Fig Q5c.
Q7- (20 marks)
1. Define “Interfacing”.
The coupling between a system under consideration and another system or between devices of a system, through which information passes.

2. For what the S&H unit is mainly used in a DDC system? Plot a basic cct. for the S&H unit that uses two buffers.
S&H is used to sample an analog signal and to store its value for some length of time for digital code conversion.

3. Name two benefits of optical isolator, and give a simple cct. which uses an optical isolator to send signal from one side to another side.
- Preventing high voltages on one side of the cct from damaging components on the other side.
- Preventing rapidly changing voltages on one side of the cct from distorting signals on the other side.

4. Define noise to a system.
Any unwanted and bad effects caused by any phenomena which lead to deviate system signals (in value, or shape) and system action from the designed or wanted ones.

5. In electrical systems, noise could spread through …wired….. or ……………wireless…. ways.
6. Most laboratories and industrial environments contain abundant electrical-noise sources, including:
   - Ac power lines
   - Heavy machinery
   - Radio and TV
7. Building a completely noise-free environment just for running tests and measurements is seldom a practical solution. Fortunately, simple devices and techniques such as (proper grounding methods), (shielded and twisted wires), (signal averaging methods), filters, and differential input Amps can control the noise in most measurements.
8. To reduce noise effect, some techniques remove extraneous noise from the signal, while others prevent noise from entering the system.
9. Say yes or no:
   - Noise is a must issue to care for in control and data acquisition systems to have them work correctly. (y)
   - Hardware, software, and theory are the three main issues in designing a microcomputer based control system (y)
10. Plot a cct. For an active 1st order low pass filter.
11. Define serial port
An asynchronous port on the computer used to connect a serial device to the computer and capable of transmitting one bit at a time.

12. What is meant by DSR in serial port?
Data Set Ready (DSR) - Modem tells the computer that it is ready to talk.

13. What are the 4 commands used to enable flow control in the serial port
RTS, CTS, DTR, DSR

14. Name 2 advantages of the serial connection.
Reduce cost, reduce noise.

15. Can I connect A/Ds and other ICs to the serial port? (Yes) . If yes would it be easy and straightforward or on the contrary? (NO)

16. In figure ( Q-7-a ) complete connections using directed arrows.

17. PCI stands for: Peripheral Components Interconnect

18. The PCI Local Bus is a high performance bus for interconnecting chips, expansion boards and processor/memory sub system.

19. PCI is a synchronous bus architecture with all data transfers being performed relative to a System clock
20. In the figure below, complete the missing signal names and phases names

Timing diagram for a read transaction on the PCI bus:

21. Give the procedure (steps) of a normal read transaction
The initiator tells the arbiter its need for a transaction (REQ), the arbiter grants (GNT), the initiator asserts FRAME, and then gives the address and bus command, the target asserts DEVSEL, transfer of data occurs when both the target and initiator are ready using TRDY and IRDY, when the transmission is complete the initiator de-asserts FRAME and the target de-asserts DEVSEL.

22. What is meant by master abort?

If the initiator never receives an active DEVSEL# it terminates the transaction in what is termed a master abort.