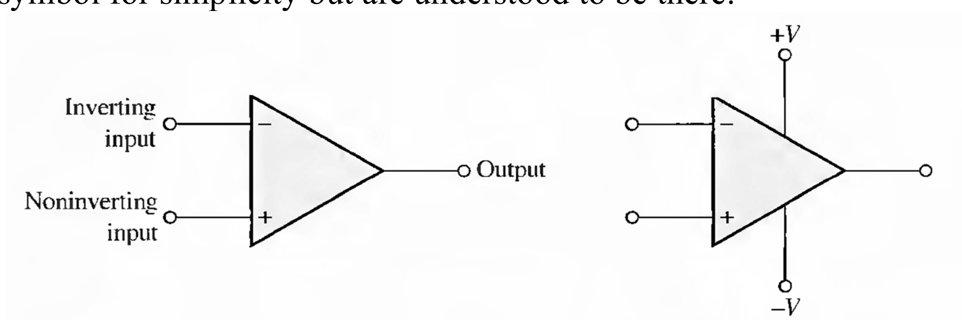
The Operational Amplifier (Op-Amp)

1.1 General Concepts:

An operational amplifier, or op-amp, is a ***very high gain*** ($A \approx \infty$) differential amplifier with ***high input impedance*** ($Z_i \approx \infty$) and ***low output impedance*** ($Z_o \approx 0$). Typical uses of the operational amplifier are to provide voltage amplitude changes (amplitude and polarity), oscillators, filter circuits, and many types of instrumentation circuits. An op-amp contains a number of differential amplifier stages to achieve a very high voltage gain.

The standard operational amplifier symbol is shown in Fig. 1-1(a). It has two input terminals, the inverting (−) input and the noninverting (+) input, and one output terminal. Each input results in either the same or an opposite polarity (or phase) output, depending on whether the signal is applied to the plus (+) or the minus (−) input.

The typical op-amp operates with two dc supply voltages, one positive and the other negative, as shown in Fig. 1-1(b). Usually these dc voltage terminals are left off the schematic symbol for simplicity but are understood to be there.



(a) (b)

Fig. 1-1

1.2 Block Diagram and Differential Amplifier of an Op-Amp:

A typical op-amp is made up of three types of amplifier circuit: a differential amplifier, a voltage amplifier, and a push-pull amplifier, as shown in Fig. 1-2. A differential amplifier is the input stage for the op-amp, It provides amplification of the difference voltage between the two inputs. The second stage is usually a class A amplifier that provides additional gain. Some op-amps may have more than one voltage amplifier stage. A push-pull class B amplifier is typically used for the output stage.

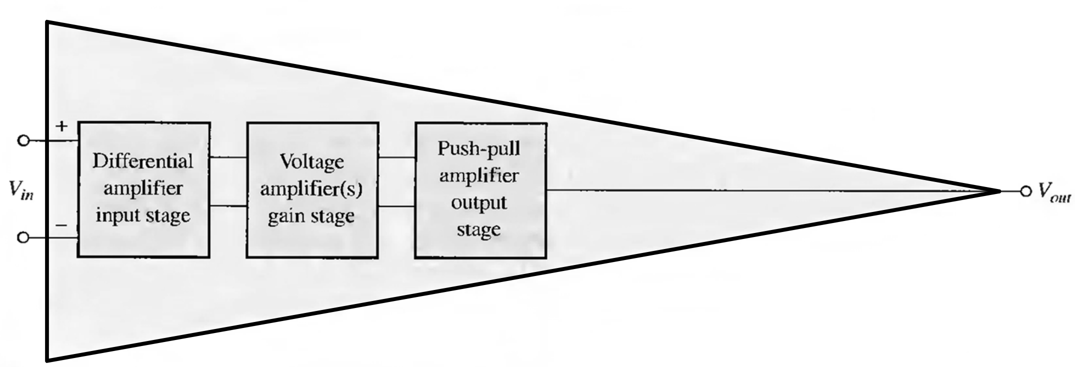
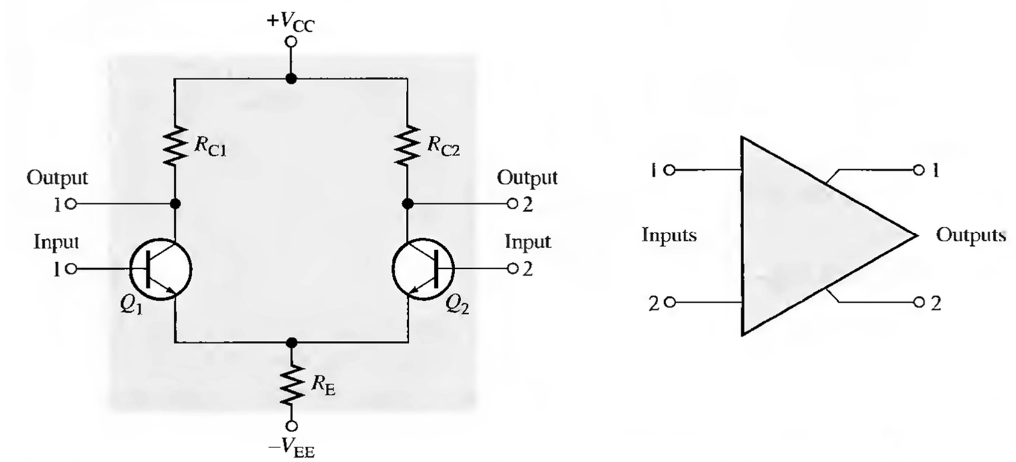


Fig. 1-2

A differential amplifier forms the input stage of operational amplifiers. The term differential comes from the amplifier's ability to amplify the difference of two input signals applied to its inputs. Only the difference in the two signals is amplified; if there is no difference, the output is zero. A basic differential amplifier circuit and its symbol are shown in Fig. 1-3. The transistors (Q_1 and Q_2) and the collector resistors (R_{C1} and R_{C2}) are carefully matched to have identical characteristics. Notice that the two transistors share a single emitter resistor, R_E.



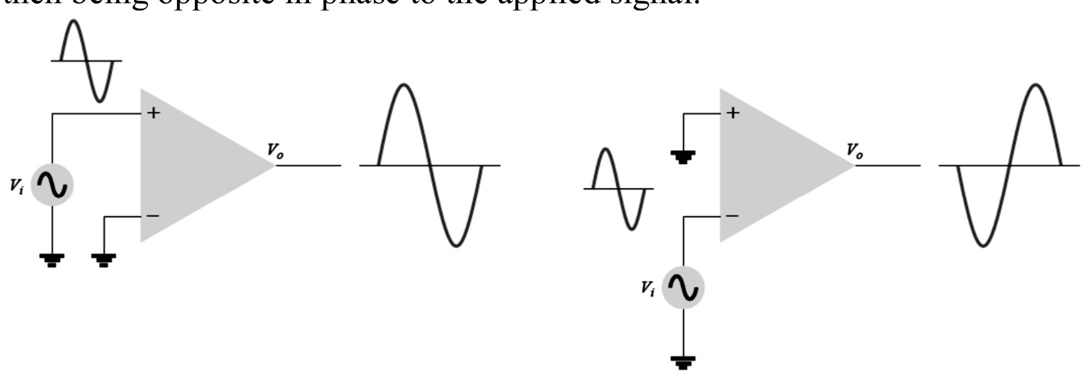
(a) (b)

Fig. 1-3

1.3 Op-Amp Operation Modes:

The differential amplifier exhibits three modes of operation based on the type of input (and/or output) signals. These modes are ***single-ended***, ***double-ended*** or ***differential***, and ***common***. Since the differential amplifier is the input stage of the op-amp, the op-amp exhibits the same modes.

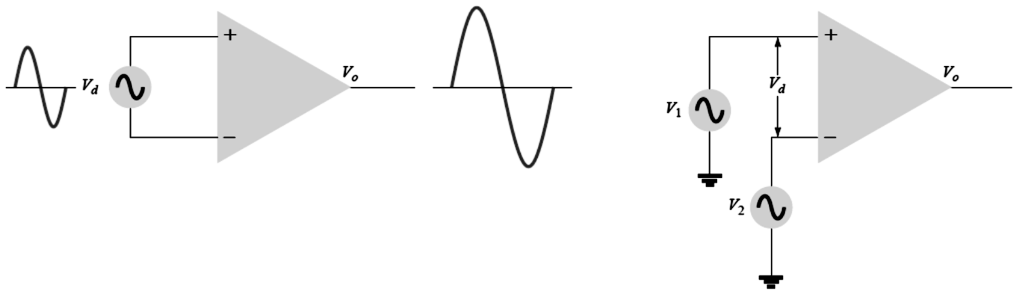
Single-Ended Input: Single-ended input operation results when the input signal is connected to one input with the other input connected to ground. Fig. 1-4 shows the signals connected for this operation. In Fig. 1-4(a), the input is applied to the plus input (with minus input at ground), which results in an output having the same polarity as the applied input signal. Fig. 1-4(b) shows an input signal applied to the minus input, the output then being opposite in phase to the applied signal.



(a) (b)

Fig. 1-4

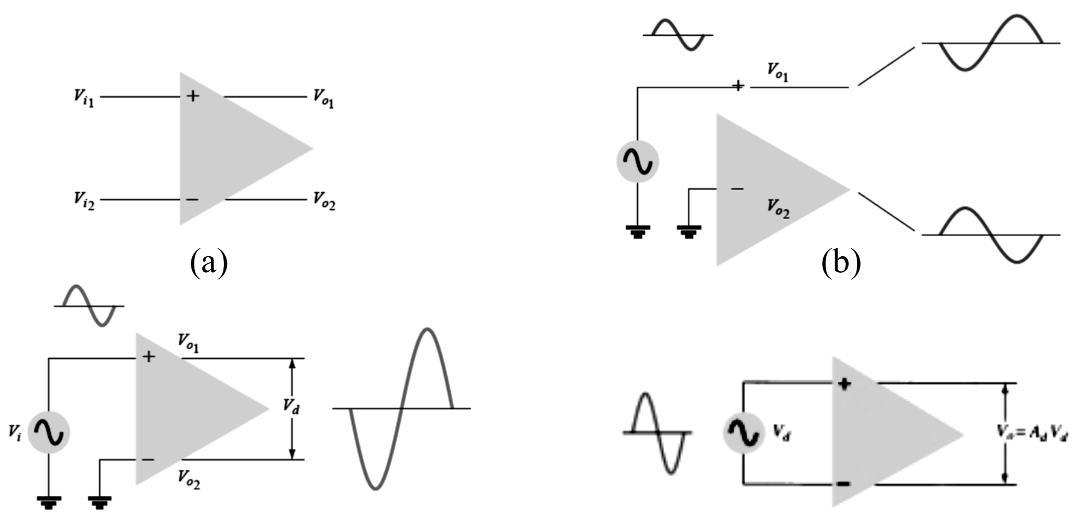
Double-Ended (Differential) Input: In addition to using only one input, it is possible to apply signals at each input-this being a double-ended operation. Fig. 1-5(a) shows an input, V_d, applied between the two input terminals (recall that neither input is at ground), with the resulting amplified output in phase with that applied between the plus and minus inputs. Fig. 1.5(b) shows the same action resulting when two separate signals are applied to the inputs, the difference signal being $V_{i1} - V_{i2}$.



(a) (b)

Fig. 1-5

Double-Ended Output: While the operation discussed so far had a single output, the op-amp can also be operated with opposite outputs, as shown in Fig. 1-6(a). An input applied to either input will result in outputs from both output terminals, these outputs always being opposite in polarity. Fig. 1-6(b) shows a single-ended input with a double-ended output. As shown, the signal applied to the plus input results in two amplified outputs of opposite polarity. Fig. 1-6(c) shows the same operation with a single output measured between output terminals (not with respect to ground). This difference output signal is $V_{o1} - V_{o2}$. The difference output is also referred to as a floating signal since neither output terminal is the ground (reference) terminal. Notice that the difference output is twice as large as either V_{o1} or V_{o2} since they are of opposite polarity and subtracting them results in twice their amplitude. Fig. 1-6(d) shows a differential input, differential output operation. The input is applied between the two input terminals and the output taken from between the two output terminals. This is fully differential operation.



(a) (b)

(c) (d)

Fig. 1-6

Common-Mode Operation: When the same input signals are applied to both inputs, common-mode operation results, as shown in Fig. 1-7. Ideally, the two inputs are equally amplified, and since they result in opposite polarity signals at the output, these signals cancel, resulting in 0-V output. Practically, a small output signal will result.

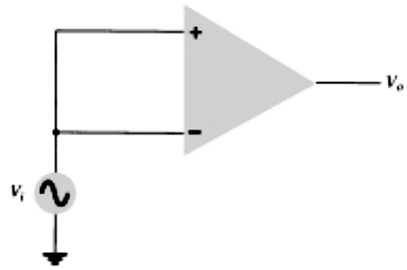


Fig. 1-7

Common-Mode Rejection: A significant feature of a differential connection is that the signals which are opposite at the inputs are highly amplified, while those which are common to the two inputs are only slightly amplified-the overall operation being to amplify the difference signal while rejecting the common signal at the two inputs. Since noise (any unwanted input signal) is generally common to both inputs, the differential connection tends to provide attenuation of this unwanted input while providing an amplified output of the difference signal applied to the inputs. This operating feature, referred to as common-mode rejection.

1.4 Common-Mode Reject Ratio (CMRR):

One of the more important features of a differential circuit connection, as provided in an op-amp, is the circuit's ability to greatly amplify signals that are opposite at the two inputs, while only slightly amplifying signals that are common to both inputs. An op-amp provides an output component that is due to the amplification of the difference of the signals applied to the plus and minus inputs and a component due to the signals common to both inputs. Since amplification of the opposite input signals is much greater than that of the common input signals, the circuit provides a common mode rejection as described by a numerical value called the common-mode rejection ratio (CMRR).

Differential Inputs: When separate inputs are applied to the op-amp, the resulting difference signal is the difference between the two inputs.

$$V_d = V_{i1} - V_{i2} \qquad [1\text{-}1]$$

Common Inputs: When both input signals are the same, a common signal element due to the two inputs can be defined as the average of the sum of the two signals.

$$V_c = \frac{1}{2}(V_{i1} + V_{i2}) \qquad [1\text{-}2]$$

Output Voltage: Since any signals applied to an op-amp in general have both in-phase and out-of phase components, the resulting output can be expressed as

$$V_o = A_d V_d + A_c V_c \qquad [1\text{-}3]$$

where A_d = differential gain, and A_c = common-mode gain of the amplifier.

Having obtained A_d and A_c, we can now calculate a value for the common-mode rejection ratio (CMRR), which is defined by the following equation:

$$\text{CMRR} = \frac{A_d}{A_c} \qquad [1\text{-}4]$$

The value of CMRR can also be expressed in logarithmic terms as

$$\text{CMRR (dB)} = 20\log_{10}\left(\frac{A_d}{A_c}\right) \qquad [1\text{-}5]$$

Exercise 1-1:

Calculate the CMRR and express it in decibel for the circuit measurements shown in Fig. 1-8.

[Answers: 666.7, 56.48 dB]

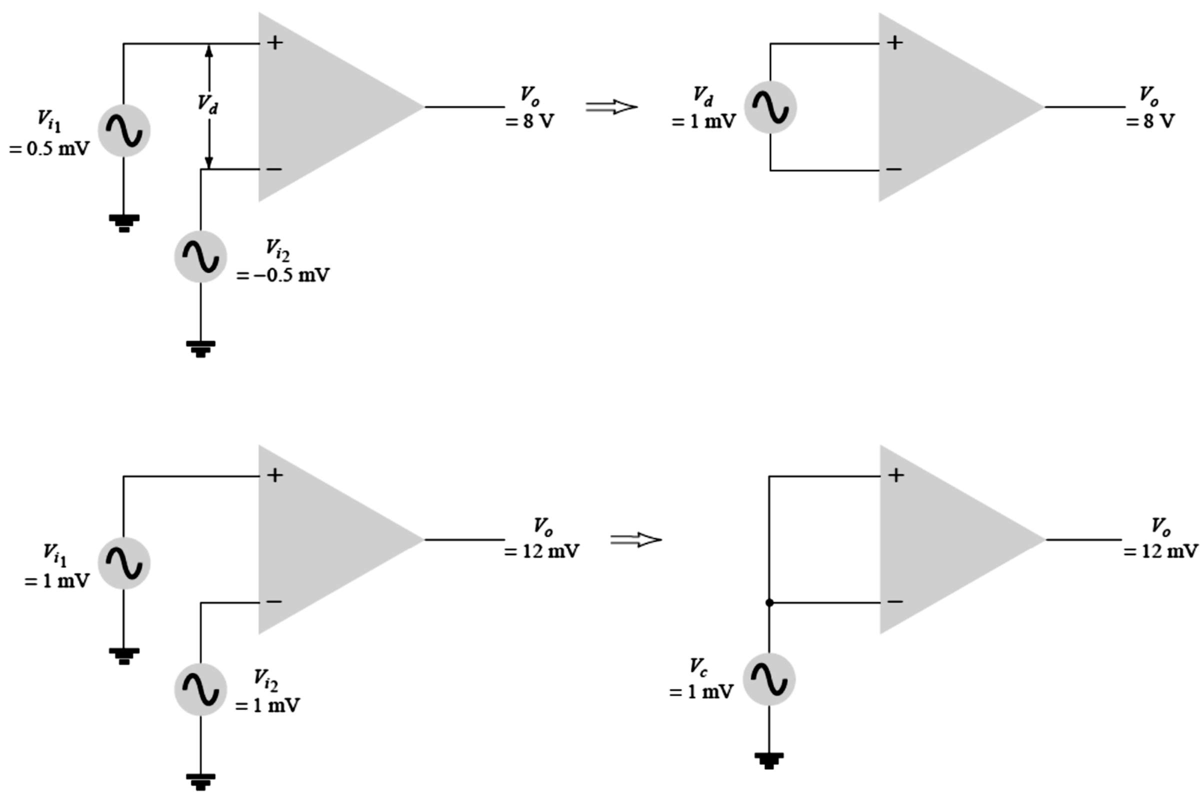


Fig. 1-8

Exercise 1-2:

Determine the output voltage of an op-amp for input voltages of V_{i1} = 150 μV, V_{i2} = 140 μV. The amplifier has a differential gain of A_d = 4000 and the value of CMRR is: (a) 100, and (b) 10^5.

[Answers: (a) 45.8 mV, (b) 40.006 mV]

1.5 The Inverting Op-Amp:

Consider the configuration shown in Fig. 1-9(a). In this very useful application of an operational amplifier, the noninverting input is grounded, v_{in} is connected through R_1 to the inverting input, and feedback resistor R_f is connected between the output and v_i^-. Since we are using the amplifier in an inverting mode, we denote the voltage gain by $-A$, $v_{in} \neq v_i^-$, we define $v_o = -Av_i^-$.

From Fig. 1-9(b); $i_1 = (v_{in} - v_i^-)/R_1$, $i_f = (v_i^- - v_o)/R_f$, $i_1 = i_f + i^-$,

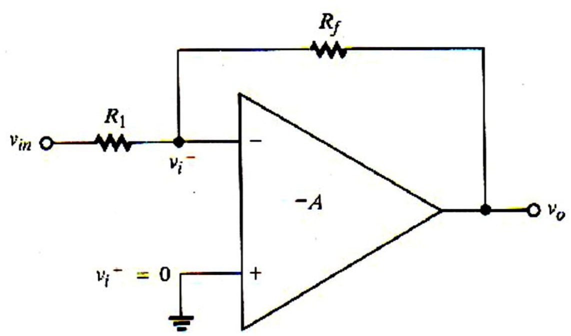
and $Z_i = \infty$ => $i^- = 0$ => $i_1 = i_f$,

or $(v_{in} - v_i^-)/R_1 = (v_i^- - v_o)/R_f$ or $\frac{v_{in}}{R_1} - \frac{v_i^-}{R_1} = \frac{v_i^-}{R_f} - \frac{v_o}{R_f}$,

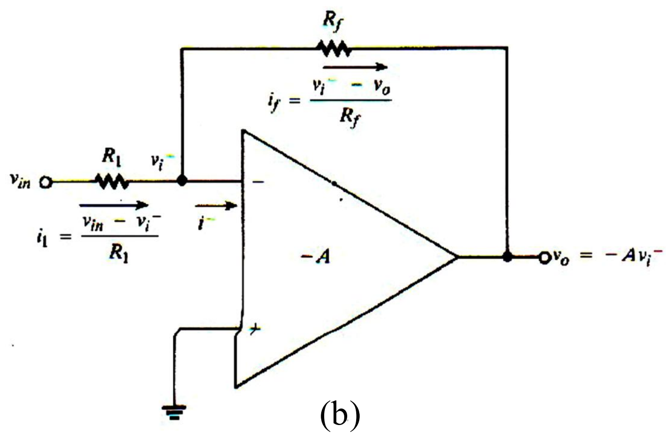
and $v_i^- = -\frac{v_o}{A}$, $|A| = \infty$ => $v_i^- = 0$ => $\frac{v_{in}}{R_1} = -\frac{v_o}{R_f}$ or

$$\frac{v_o}{v_{in}} = -\frac{R_f}{R_1} \qquad [1\text{-}6]$$

In Eqn. [1-6] the gain is negative, signifying that the configuration is an inverting amplifier, also the magnitude of v_o/v_{in} depends only on the ratio of the resistor values. The gain v_o/v_{in} is a ***closed-loop gain*** of the amplifier, while A is called the ***open-loop gain***.



(a)



(b)

Fig. 1-9

Exercise 1-3:

Assuming that the operational amplifier in Fig. 1-10 is ideal, find

(a) the rms value of v_o when v_{in} is 1.5 V rms,
(b) the rms value of the current in the 25-kΩ resistor when v_{in} is 1.5 V rms, and
(c) the output voltage when $v_{in} = -0.6$ V dc.

[Answers: (a) 8.25 V rms, (b) 60 μA rms, (c) 3.3 V dc]

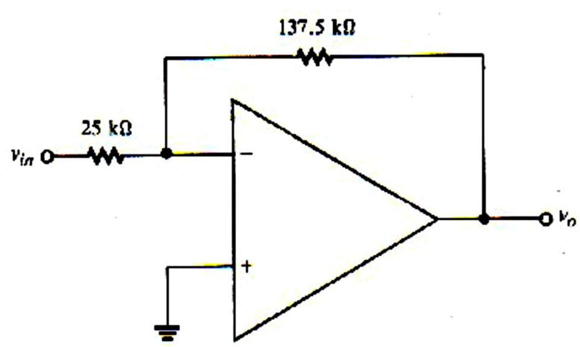


Fig. 1-10

1.6 The Noninverting Op-Amp:

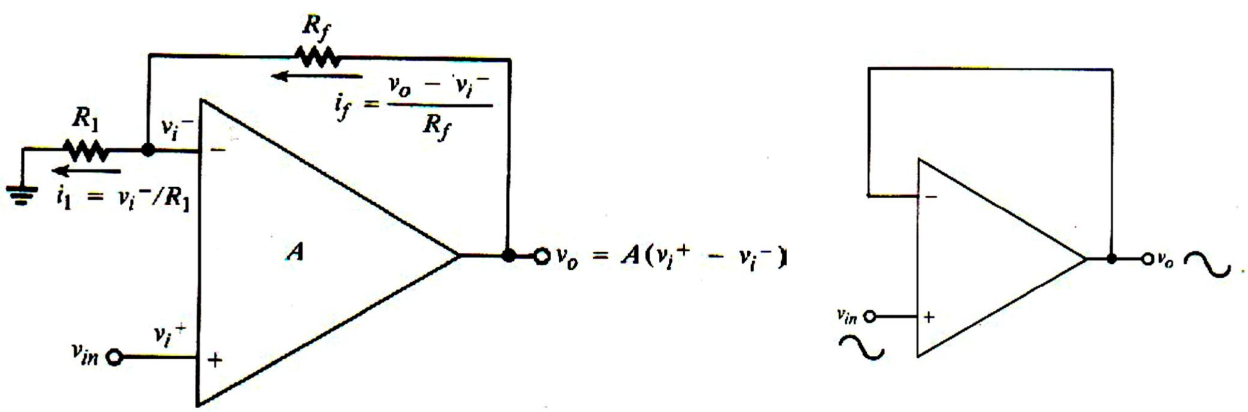
Fig. 1-11(a) shows another useful application of an operational amplifier, called the noninverting configuration. The input signal v_{in} is connected directly to the noninverting input and R_1 is connected from the inverting input to ground. Under the ideal assumption of infinite input impedance, no current flows into the inverting input, so $i_1 = i_f$.

Thus, $\frac{v_i^-}{R_1} = \frac{v_o - v_i^-}{R_f}$ and $v_o = A(v_i^+ - v_i^-)$ => $v_i^- = v_i^+ - v_o/A$,

$|A| = \infty$ => $v_o/A = 0$ => $v_i^- = v_i^+$ and $\frac{v_i^+}{R_1} = \frac{v_o - v_i^+}{R_f}$, where $v_i^+ = v_{in}$ =>

$$\frac{v_o}{v_{in}} = 1 + \frac{R_f}{R_1} = \frac{R_1 + R_f}{R_1} \qquad [1\text{-}7]$$

Eqn. [1-7] shows that the closed-loop gain of the noninverting amplifier, like that of the inverting amplifier, depends only on the values of external resistors. Fig. 1-11(b) shows a special case of noninverting amplifier, used in applications where power gain and impedance isolation are of primary concern. When $R_f = 0$ and $R_1 = \infty$, so the closed-loop gain is $v_o/v_{in} = 1 + R_f/R_1 = 1$. This configuration is called a ***voltage follower*** because v_o has the same magnitude and phase as v_{in}. It has large input impedance and small output impedance, and is used as a ***buffer*** amplifier between a high-impedance source and a low-impedance load.



(a) (b)

Fig. 1-11

Exercise 1-4:

In a certain application, a signal source having 60 kΩ of source impedance, R_S, produces a 1-V-rms signal. This signal must be amplified to 2.5 V rms and drive a 1-kΩ load. Assuming that the phase of the load voltage is of no concern, design an operational amplifier circuit for the application.

Hint: Choose, arbitrarily, input resistor, R_1 = 100 kΩ and find feedback resistor, R_f. Since phase is of no concern and the required voltage gain is greater than 1, we can use either an inverting or noninverting amplifier.

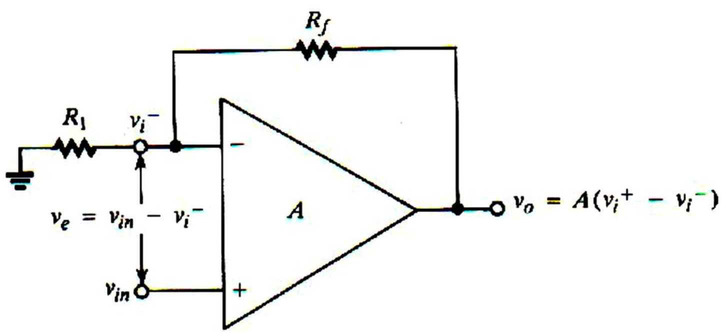
[Answers: $R_{f\,(inverting)}$ = 400 kΩ, $R_{f\,(noninverting)}$ = 150 kΩ]

1.7 Op-Amp Analysis using Feedback Theory:

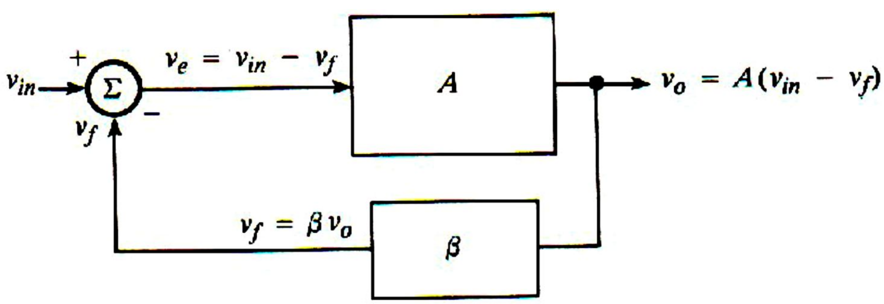
We have seen that we can control the closed-loop gain v_o/v_{in} of an operational amplifier by introducing feedback through external resistor combinations. We wish now to examine the feedback mechanism in detail and discover some other important consequences of its use. Feedback theory is widely used to study the behavior of electronic components as well as complex systems in many different technical fields, so it is important to develop an appreciation and understanding of its underlying principles.

1.7.1 Feedback in the Noninverting Op-Amp:

Fig. 1-12 shows the noninverting configuration along with an equivalent block diagram on which we can identify the signal and feedback paths. "A" represents the amplifier and its open-loop gain, "β" is called the feedback ratio and represents the output voltage that is fed back to the input. $v_e = v_{in} - v_f$. v_e is often called the error voltage. The feedback voltage $v_f = \beta v_o$ corresponds to v_i^- in the amplifier circuit. Since the feedback voltage subtracts from the input voltage, the amplifier is said to have negative feedback.



(a)



(b)

Fig. 1-12

With reference to Fig. 1-12(b), we see that $v_o = A(v_{in} - v_f)$, $v_f = \beta v_o$ => $v_o = A(v_{in} - \beta v_o) = Av_{in} - A\beta v_o$ or $v_o(1 + A\beta) = Av_{in}$ =>

$$\frac{v_o}{v_{in}} = \frac{A}{1+A\beta} = \frac{1/\beta}{1+1/A\beta} \qquad [1\text{-}8]$$

Form a voltage divider across v_o, $v_i^- = \left(\frac{R_1}{R_1+R_f}\right) v_o$, $v_i^- = v_f = \beta v_o$ =>

$$\beta = \frac{R_1}{R_1+R_f} \text{ (noninverting op-amp)} \qquad [1\text{-}9]$$

Substituting Eqn. [1-9] into Eqn. [1-8], we find

$$\frac{v_o}{v_{in}} = \frac{(R_1+R_f)/R_1}{1+1/A\beta} = \frac{(R_1+R_f)/R_1}{1+(R_1+R_f)/AR_1} \qquad [1\text{-}10]$$

when $A = \infty$ =>

$$\frac{v_o}{v_{in}} = \frac{1}{\beta} = \frac{R_1+R_f}{R_1} = 1 + \frac{R_f}{R_1} \qquad [1\text{-}11]$$

Eqn. [1-11] is exactly the same result we obtained from Eqn. [1-7].

Negative feedback improves the performance of an amplifier in several ways. In the case of the noninverting amplifier, it can be shown that the input resistance seen by the signal source (looking directly into the + terminal) is

$$r_{if} = r_{in} = (1 + A\beta)r_{id} \approx A\beta r_{id} \qquad [1\text{-}12]$$

where r_{id} is the differential input resistance of the amplifier.

The closed-loop output resistance of the noninverting amplifier is also improved by negative feedback:

$$r_{of} = r_o(stage) = \frac{r_o}{1+A\beta} \approx \frac{r_o}{A\beta} \qquad [1\text{-}13]$$

where r_o is the open-loop output resistance of the amplifier.

Exercise 1-5:

Find the closed-loop gain of the amplifier in Fig. 1-13 when (a) A = ∞, (b) A = 10^6, and (c) A = 10^3.

[Answers: (a) 10, (b) 9.9990, (c) 9.90099]

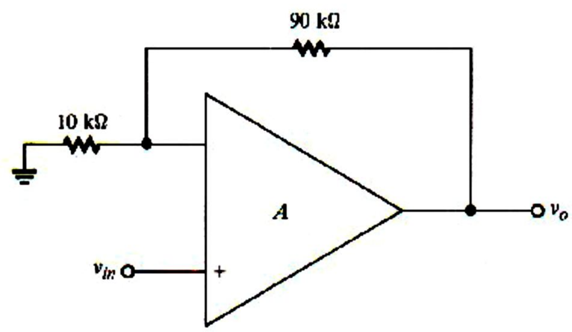


Fig. 1-13

Exercise 1-6:

An operational amplifier has open-loop gain $A = 10^4$. Compare its closed-loop gain with that of an ideal amplifier when (a) $\beta = 0.1$, and (b) $\beta = 0.001$.

[Answers: (a) 9.99, (b) 909.09]

Exercise 1-7:

A noninverting op-amp has open-loop gain $A = 10^5$, feedback ratio $\beta = 0.01$, differential input resistance $r_{id} = 20$ kΩ, and open-loop output resistance $r_o = 75$ Ω. Find the closed-loop input (r_{if}) and output (r_{of}) resistances of the amplifier.

[Answers: 20 MΩ, 0.075 Ω]

1.7.2 Feedback in the Inverting Op-Amp:

To investigate the effect of open-loop gain A and feedback ratio β on the closed-loop gain of the inverting amplifier, let us recall Fig. 1-9(b):

$$\frac{v_{in}}{R_1} - \frac{v_i^-}{R_1} = \frac{v_i^-}{R_f} - \frac{v_o}{R_f} \text{ and } v_i^- = -\frac{v_o}{A} \Rightarrow \frac{v_{in}}{R_1} + \frac{v_o}{AR_1} = -\frac{v_o}{AR_f} - \frac{v_o}{R_f} \text{ or}$$

$$v_o + \frac{v_o}{A} + \frac{v_o R_f}{AR_1} = -\frac{v_{in} R_f}{R_1} \text{ or } v_o\left(1 + \frac{R_1 + R_f}{AR_1}\right) = -\frac{v_{in} R_f}{R_1} \Rightarrow$$

$$\frac{v_o}{v_{in}} = \frac{-R_f/R_1}{1+(R_1+R_f)/AR_1} \qquad [1\text{-}14]$$

Once again, when $A = \infty$, we see that the closed-loop gain reduces to the ideal amplifier value, $-R_f/R_1$ (Eqn. [1-6]). By the superposition principle, we can analyze the contribution of the feedback source by grounding all other signal sources. When this is done, as shown in Fig. 1-14, we see that the feedback voltage in both configurations is developed across R_1 and R_f by voltage divider, and $\beta = R_1/(R_1+R_f)$ in both cases. In view of this fact, we can write Eqn. [1-14] as

$$\frac{v_o}{v_{in}} = \frac{-R_f/R_1}{1+1/A\beta} \qquad [1\text{-}15]$$

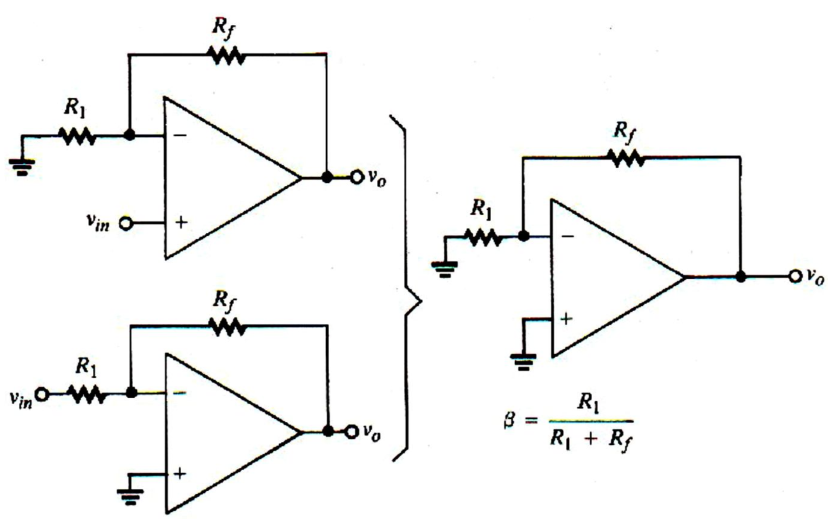


Fig. 1-14

Towards developing a feedback model for the inverting amplifier, consider the block diagram shown in Fig. 1-15. It is quite similar to Fig. 1-12(b) for the noninverting amplifier, except that we now denote the open loop gain by $-A$, v represents an arbitrary input voltage, rather than v_{in}. As shown in the figure;

$$v_o = -A(v + \beta v_o) \text{ or } \frac{v_o}{v} = \frac{-A}{1+A\beta} = \frac{-1/\beta}{1+1/A\beta} \Rightarrow \frac{v_o}{v} = \frac{-(R_1+R_f)/R_1}{1+1/A\beta}.$$

Multiplying the right side by the factor $R_f/(R_1+R_f)$, we would obtain

$$\frac{v_o}{v} = \left[\frac{\frac{-(R_1+R_f)}{R_1}}{1+1/A\beta}\right]\frac{R_f}{R_1+R_f} = \frac{-R_f/R_1}{1+1/A\beta} \qquad [1\text{-}16]$$

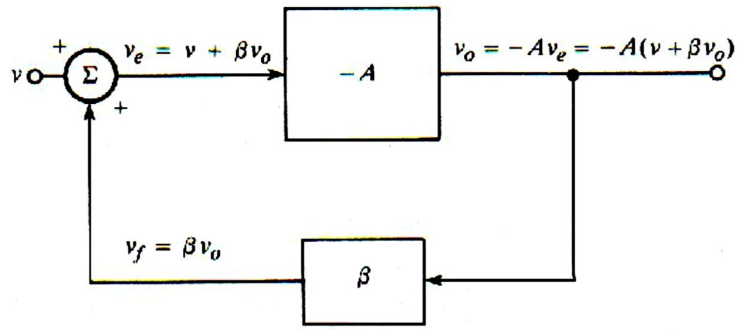


Fig. 1-15

Eqn. [1-16] gives us exactly the same result (Eqn. [1-15] with $v_{in} = v$) that we obtain for the inverting amplifier. Therefore, we modify the block-diagram model in Fig. 1-15 by adding a block that multiplies the input by $R_f/(R_1 + R_f)$. The complete feedback model is shown in Fig. 1-16. As can be seen, the loop gain for the inverting amplifier is $A\beta$, the same as that for the noninverting amplifier.

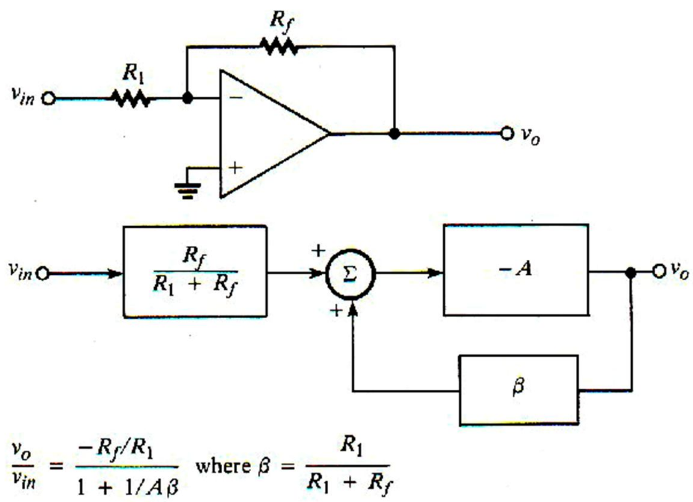


Fig. 1-16

It can be shown that the input resistance seen by the signal source driving the inverting amplifier is

$$r_{if} = r_{in} = R_1 + \frac{R_f}{1+A} \approx R_1 \qquad [1\text{-}17]$$

As with the noninverting amplifier, the output resistance of the inverting amplifier is decreased by the negative feedback. In fact, the relationship between output resistance and loop gain is the same for both:

$$r_{of} = r_o(stage) = \frac{r_o}{1+A\beta} \approx \frac{r_o}{A\beta} \qquad [1\text{-}18]$$

In closing our discussion of feedback theory, we should note once again that the same relationship between actual and ideal closed-loop gain applies to inverting and noninverting amplifiers. This relationship is

$$actual\ \frac{v_o}{v_{in}} = \frac{ideal\ closed{-}loop\ gain}{1+1/A\beta} \qquad [1\text{-}19]$$

where (ideal closed-loop gain) is the closed-loop gain v_o/v_{in} that would result if the amplifier were ideal ($A = \infty$). We saw this relationship in Eqn. 1-10 and Eqn. 1-15, repeated here:

$$\frac{v_o}{v_{in}} = \frac{(R_1+R_f)/R_1}{1+1/A\beta} \qquad \text{(noninverting op-amp)}$$

$$\frac{v_o}{v_{in}} = \frac{-R_f/R_1}{1+1/A\beta} \qquad \text{(inverting op-amp)}$$

In both cases, the numerator is the closed-loop gain that would result if the amplifier were ideal. Also in both cases, the greater the value of the loop gain $A\beta$, the closer the actual closed-loop gain is to the ideal closed-loop gain.

Exercise 1-8:

The amplifier shown in Fig. 1-17 has open-loop gain equal to −2500 and open-loop output resistance 100Ω. Find

(a) the magnitude of the loop gain ($A\beta$),
(b) the closed-loop gain (v_o/v_{in}),
(c) the input resistance (r_{if}) seen by v_{in}, and
(d) the closed-loop output resistance (r_{of}).

[Answers: (a) 24.75, (b) − 96.12 (≈ − 100), (c) 1560 Ω, (d) 3.88 Ω]

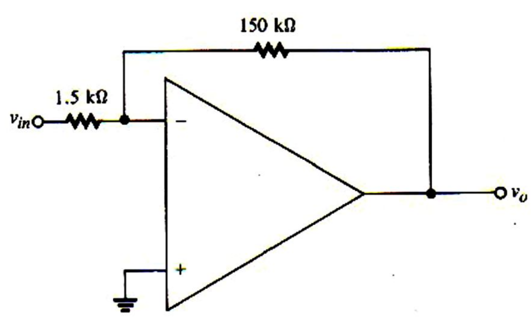


Fig. 1-17

1.8 Frequency Response and Stability:

When the word ***stability*** is used in high-gain amplifier, it means behaving like an amplifier rather than like an oscillator. an operational amplifier has very high gain, so precautions must be taken in its design to ensure that it does not oscillate (an oscillator is a device that generates an ac signal because of positive feedback), large gains at high frequencies tend to make an amplifier unstable, to ensure stable operation, most operational amplifiers have internal compensation circuitry that causes the open-loop gain to diminish with increasing frequency. This reduction in gain is called rolling-off the amplifier. The usable frequency range rolls off at the rate of − 20 dB/decade, or − 6 dB/octave.

1.9 The Gain-Bandwidth Product:

Fig. 1-18 shows frequency response characteristic for the open-loop gain of an operational amplifier, f_c is the cutoff frequency (the frequency at which the gain A falls to $\sqrt{2}/2$ times its low-frequency or dc value, A_o). The slope of the single-pole response, − 20 dB/decade, is −1. The frequency at which the β falls to the value 1 (unity) is given by $f_T = \beta_m f_\beta$, where β_m is the low frequency β (or h_{fe}) and f_B is the β cutoff frequency. Using exactly the same approach;

$$f_t = A_o f_c \qquad [1\text{-}20]$$

where f_t = the unity-gain frequency, the frequency at which the gain equals 1, A_o = the low-frequency, or dc, value of the open-loop gain, and f_c = the cutoff frequency, or 3-dB frequency, of the open-loop gain.

Since the amplifier is dc (lower cutoff frequency = 0), the bandwidth equals f_c. The term $A_o f_c$ in Eqn. [1-20] is called the ***gain-bandwidth product*** or for its equivalent, the ***unity-gain frequency***.

The relationship between closed-loop bandwidth (BW_{CL}) and the gain-bandwidth product is closely approximated by

$$BW_{CL} = f_t\beta = A_o f_c \beta \qquad [1\text{-}21]$$

where β is the feedback ratio.

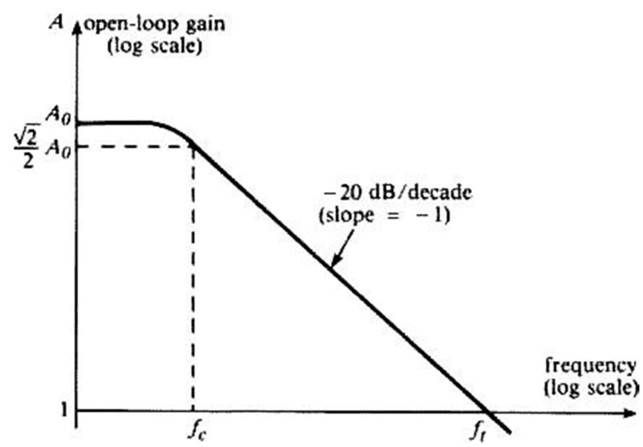
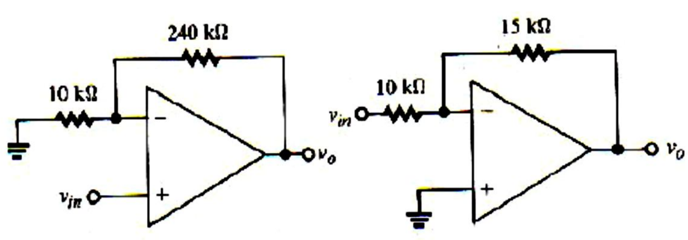


Fig. 1-18

Exercise 1-9:

Each of the amplifiers shown in Fig. 1-19 has an open-loop, gain-bandwidth product equal to 1 × 10^6. Find the cutoff frequencies in the closed-loop configurations shown.

[Answers: (a) 40 kHz, (b) 400 kHz]



(a) (b)

Fig. 1-19

Exercise 1-10:

With reference to the amplifier whose frequency response is shown in Fig 1-20, find

(a) the unity-gain frequency,
(b) the gain-bandwidth product,
(c) the bandwidth when the feedback ratio is 0.02, and
(d) the closed-loop gain at 0.4 MHz when the feedback ratio is 0.04.

[Answers: (a) 1 MHz, (b) 10^6, (c) 20 kHz, (d) 2.5]

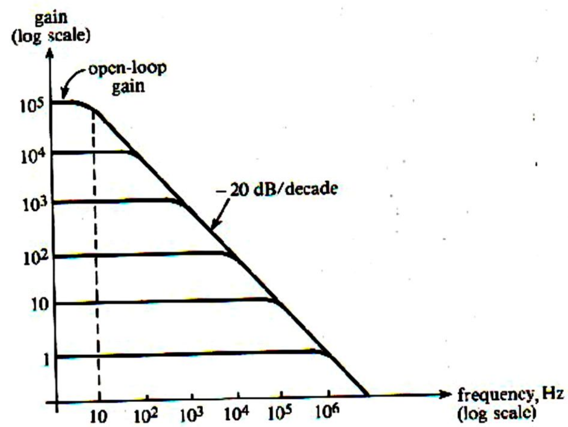


Fig. 1-20

1.10 Slew Rate:

As mentioned previously, the internal compensation circuitry used to ensure amplifier stability also affects the frequency response and places a limit on the maximum operating frequency. The capacitor(s) in this compensation circuitry limit amplifier performance because when the amplifier is driven by pulse-type signal, the capacitance must charge and discharge rapidly in order for the output to keep up with the input. Since the voltage across a capacitor cannot be changed instantaneously, there is an inherent limit on the rate at which the output voltage can change. The maximum possible rate at which an amplifier's output voltage can change, in volts per second, is called its ***slew rate***.

It is not possible for any waveform, input or output, to change from one level to another in zero time. An instantaneous change corresponds to an infinite rate of change, which is not realizable in any physical system. Therefore, in our investigation of performance limitations imposed by an amplifier's slew rate, we need only concern ourselves with inputs that undergo a total change in voltage, ΔV, over some nonzero time interval, Δt. For simplicity, we will assume that the change is linear with respect to time, that is, it is a ramp-type waveform, as illustrated in Fig. 1-21. The rate of change of this kind of waveform is the change in voltage divided by the length of time that it takes for the change to occur:

$$rate\ of\ change = \frac{V_2 - V_1}{t_2 - t_1} = \frac{\Delta V}{\Delta t}\ \text{volts/seconds} \qquad [1\text{-}22]$$

Since the value specified for the slew rate of an amplifier is the maximum rate at which its output can change, we cannot drive the amplifier with any kind of input waveform that would require the output to exceed that rate. Finally, the maximum frequency at which an amplifier can be operated depends on both the bandwidth and the slew rate.

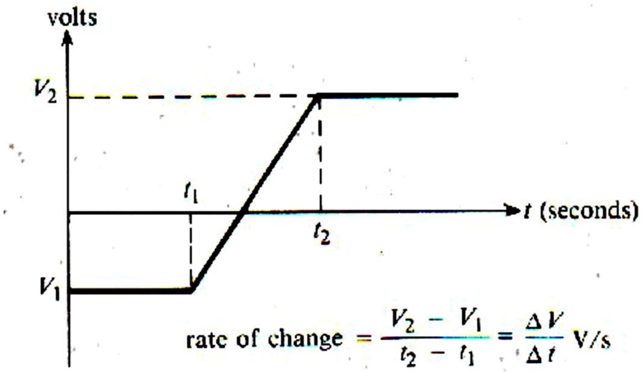


Fig. 1-21

Exercise 1-11:

The operational amplifier in Fig. 1-22 has a slew rate specification of 0.5 V/µs. If the input is the ramp waveform shown, what is the maximum closed-loop gain that the amplifier can have without exceeding its slew rate? determine the output levels corresponding to the input levels and verify the specified slew rate.

[Answers: 12.5, +2.5 V/–7.5 V, 0.5 V/µs]

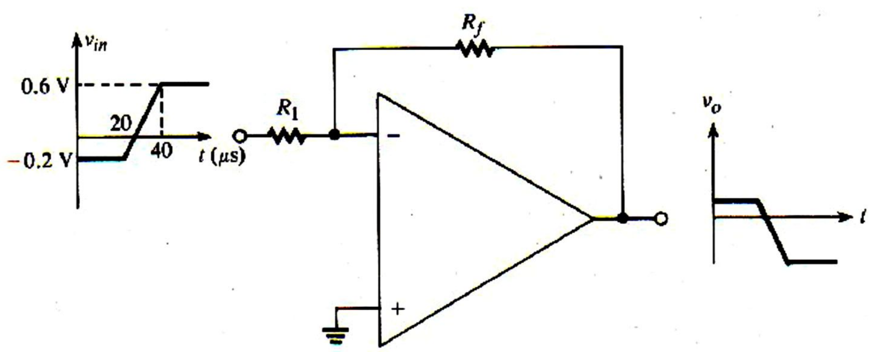


Fig. 1-22

1.11 Offset Currents and Voltages:

One of the characteristics of an ideal operational amplifier is that it has zero output voltage when both inputs are 0 volts (grounded). This characteristic is particularly important in applications where dc or low-frequency signals are involved. If the output is not 0 when the inputs are 0, then the output will not be at its correct dc level when the input is a dc level other than 0. The actual value of the output voltage when the inputs are 0 is called the ***output offset voltage***.

Manufacturers do not generally specify output offset because, the offset level depends on the closed-loop gain that a user designs through choice of external component values. Instead, input offsets are specified, and the designer can use these values to compute the output offset that results in a particular application. Output offset voltages are the result of two distinct input phenomena: ***input bias currents*** and ***input offset voltage***.

1.11.1 Input Offset Current:

We know that some dc base current (I_B) must flow when a transistor is properly biased, although its small its flowing through the external resistors produces a dc input voltage that in turn creates an output offset. To reduce the effect of bias currents (I_B^+ and I_B^-), a compensating resistor R_c, as shown in Fig. 1-23, is connected in series with the noninverting (+) terminal of the amplifier (R_c provide a dc path to ground, so if a signal is capacitor coupled to the + input, R_c must be connected between the + input and ground). The proper choice of the value of R_c will minimize the output offset voltage due to bias current. Fig. 1-24(a) shows the equivalent circuit of Fig. 1-23. Here, the bias currents are represented by current sources having resistances R_1 and R_c. Also, Fig. 1-24(b) shows the same circuit when the current sources are replaced by their Thevenin equivalent voltage sources.

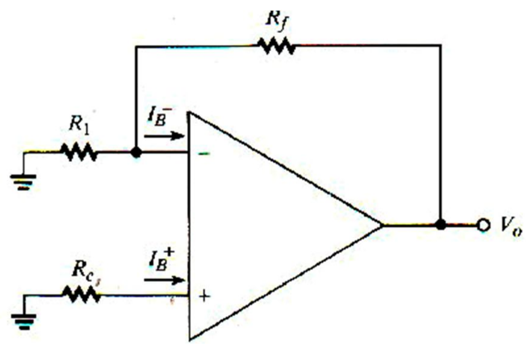
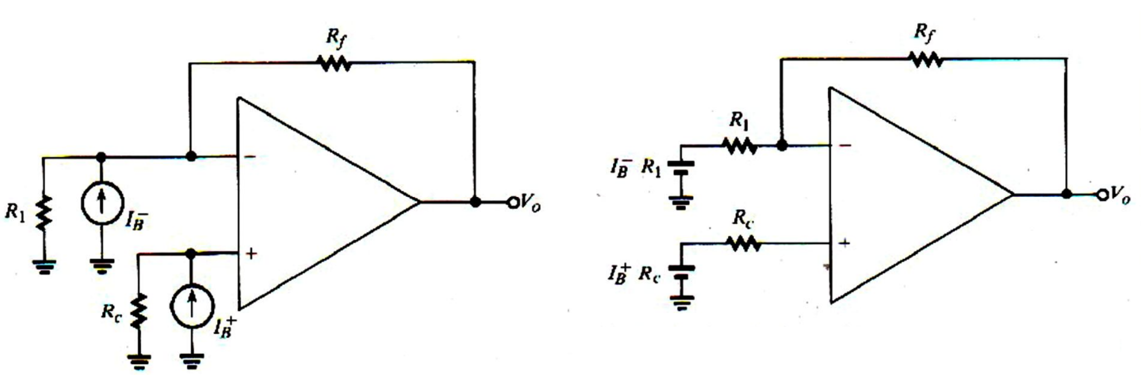


Fig. 1-23



(a) (b)

Fig. 1-24

Using Fig. 1-24(b), we can apply the superposition principle to determine the output offset voltage due to each input source acting alone and then combining the results:

$$V_{o1} = I_B^- R_1 \left(\frac{-R_f}{R_1}\right) = -I_B^- R_f \quad \text{and} \quad V_{o2} = I_B^+ R_c \left(\frac{R_f + R_1}{R_1}\right) \Rightarrow$$

$$V_{OS}(I_B) = V_{o1} + V_{o2} = I_B^+ R_c \left(\frac{R_f + R_1}{R_1}\right) - I_B^- R_f \qquad [1\text{-}23]$$

$$I_B^+ = I_B^- = I_{BB} \Rightarrow V_{OS}(I_B) = I_{BB}\left[R_c \left(\frac{R_f + R_1}{R_1}\right) - R_f\right] = 0 \Rightarrow$$

$$R_c \left(\frac{R_f + R_1}{R_1}\right) - R_f = 0 \Rightarrow R_c = \frac{R_f}{(R_f + R_1)/R_1}$$

$$R_c = \frac{R_f R_1}{R_f + R_1} = R_f \| R_1 \qquad [1\text{-}24]$$

Eqn. [1-24] reveals the very important result that output offset due to input bias currents can be minimized by connecting a resistor R_c having value $R_1 \| R_f$ in series with the noninverting input. We can compute the exact value of $V_{OS}(I_B)$ when $R_c = R_1 \| R_f$ by substituting this value of R_c back into Eqn. [1-23];

$$V_{OS}(I_B) = I_B^+(R_1 \| R_f)\left(\frac{R_f + R_1}{R_1}\right) - I_B^- R_f \quad \text{or}$$

$$V_{OS}(I_B) = I_B^+\left(\frac{R_1 R_f}{R_1 + R_f}\right)\left(\frac{R_f + R_1}{R_1}\right) - I_B^- R_f \quad =>$$

$$V_{OS}(I_B) = (I_B^+ - I_B^-)R_f \qquad [1\text{-}25]$$

Eqn. [1-25] shows the offset voltage is proportional to the difference between I_B^+ and I_B^- when $R_c = R_1 \| R_f$. The equation confirms the fact that $V_{OS} = 0$ if I_B^+ exactly equals I_B^-. The quantity $(I_B^+ - I_B^-)$ is called the input offset current and is often quoted in manufacturers specifications. Letting the input offset current $(I_B^+ - I_B^-)$ be designed by I_{io}, we have,

$$V_{OS}(I_B) = I_{io} R_f \quad \text{when} \quad R_c = R_1 \| R_f$$

$V_{OS}(I_B)$ may be either positive or negative, depending on whether $I_B^+ > I_B^-$ or vice versa, so a more useful form is

$$|V_{OS}(I_B)| = |I_{io}| R_f \quad \text{when} \quad R_c = R_1 \| R_f \qquad [1\text{-}26]$$

Manufacturers specifications always give a positive value for I_{io} (absolute value). From Eqn. [1-26] the output offset is directly proportional to R_f. For that reason, small resistance values should be used when offset is a critical consideration. Another common manufacturers specification is called input bias current, I_B. By convention, I_B is the average of I_B^+ and I_B^-;

$$I_B = \frac{I_B^+ + I_B^-}{2}$$

I_B typically much larger than I_{io} because I_B is on the same order of magnitude as I_B^+ and I_B^-, while I_{io} is the difference between the two. Given values for I_B and I_{io}, we can find I_B^+ and I_B^-, provided we know which is the larger:

$$\left.\begin{array}{l} I_B^+ = I_B + 0.5|I_{io}| \\ I_B^- = I_B - 0.5|I_{io}| \end{array}\right\} (I_B^+ > I_B^-) \quad \text{and}$$

$$\left.\begin{array}{l} I_B^+ = I_B - 0.5|I_{io}| \\ I_B^- = I_B + 0.5|I_{io}| \end{array}\right\} (I_B^+ < I_B^-) \qquad [1\text{-}27]$$

Exercise 1-12:

Given $I_B = \frac{I_B^+ + I_B^-}{2}$ and $|I_{io}| = |I_B^+ - I_B^-|$, solve equations simultaneously to show that

(a) when $I_B^+ > I_B^-$, $I_B^+ = I_B + 0.5|I_{io}|$ and $I_B^- = I_B - 0.5|I_{io}|$, and

(b) when $I_B^+ < I_B^-$, $I_B^+ = I_B - 0.5|I_{io}|$ and $I_B^- = I_B + 0.5|I_{io}|$.

Hint: When $I_B^+ > I_B^-$, $|I_B^+ - I_B^-| = I_B^+ - I_B^-$.

Exercise 1-13:

The specifications for the operational amplifier in Fig. 1-25 state that the input bias current (I_B) is 80 nA and that the input offset current (I_{io}) is 20 nA.

(a) Find the optimum value for R_c.
(b) Find the magnitude of the output offset voltage due to bias currents when R_c equals its optimum value.
(c) Assuming that $I_B^+ > I_B^-$, find the magnitude of the output offset voltage when $R_c = 0$.

[Answers: (a) 9.09 kΩ, (b) 2 mV, (c) 7 mV]

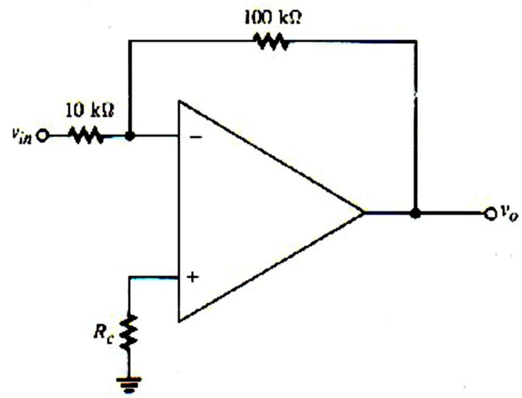


Fig. 1-25

1.11.2 Input Offset Voltage:

Another input phenomenon that contributes to output offset voltage is an internally generated potential difference that exists because of imperfect matching of the input transistors. This potential may be due to a difference between the V_{BE} drops of the transistors in the input differential stage of a BJT amplifier. Called ***input offset voltage***, the net effect of this potential difference is the same as if a small dc voltage source were connected to one of the inputs (as shown in Fig. 1-26). The output offset voltage when the input is V_{io} is given by

$$V_{OS}(V_{io}) = V_{io}\left(\frac{R_f + R_1}{R_1}\right) = \frac{V_{io}}{\beta} \qquad [1\text{-}28]$$

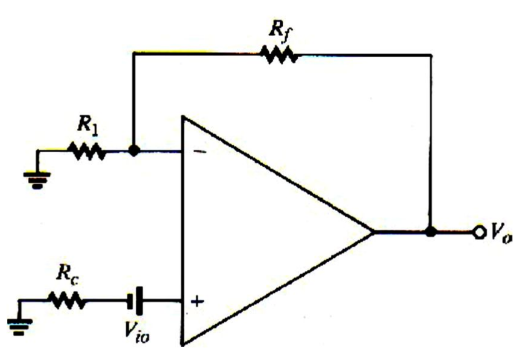


Fig. 1-26

Exercise 1-14:

The specifications for the amplifier in Exercise 1-13 state that the input offset voltage is 0.8 m V. Find the output offset due to this input offset.

[Answer: 8.8 mV]

1.1.3 The Total Output Voltage:

We have seen that output offset voltage is a function of two distinct input characteristics: input bias currents and input offset voltage. It is good design practice to assume a ***worst-case situation***, in which the two offsets have the same polarity and reinforce each other, for the worst-case situation, we assume that the total offset is the sum of the respective magnitudes:

$$|V_{OS}| = |V_{OS}(I_B)| + |V_{OS}(V_{io})| \quad \text{(worst case)} \qquad [1\text{-}29]$$

Exercise 1-15:

The operational amplifier in Fig. 1-27 has the following specifications: input bias current (I_B) = 100 nA; input offset current (I_{io}) = 20 nA; input offset voltage (V_{io}) = 0.5 mV. Find the worst-case output offset voltage. Consider the two possibilities $I_B^+ > I_B^-$ and vice versa.

Hint: First check to see if the 10 kΩ resistor in series with the noninverting input has the optimum value of a compensating resistor (R_C).

[Answers: R_c is not optimum, $I_B^{+/-}$ = 110/90 nA (vice versa), $V_{OS}(I_B)$ = −0.15/−2.85 mV, $V_{OS}(V_{io})$ = 3 mV, V_{OS} = 5.85 mV]

Exercise 1-16:

Assuming worst-case conditions at 25°C with the maximum value of input offset current (I_{io}) = 200 nA and the maximum value of input offset voltage (V_{io}) = 5 mV, determine the total output offset voltage $|V_{OS}|$, in connection with the μA741 op-amp circuit shown in Fig. 1-28.

Hint: Check the optimum value of a compensating resistor (R_C).

[Answer: 90.1 mV]

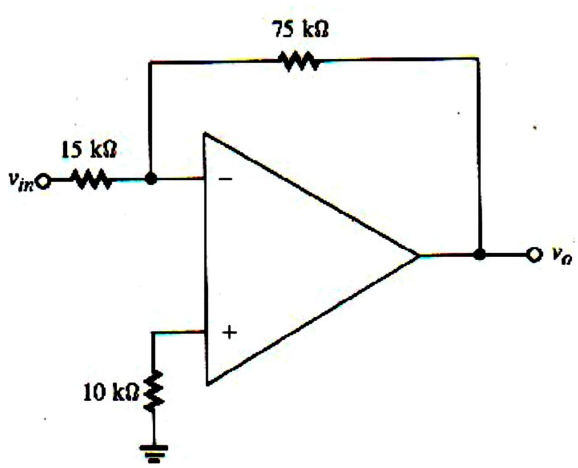


Fig. 1-27

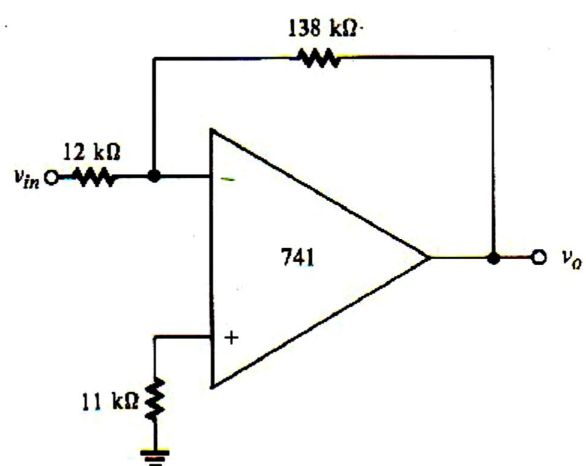


Fig. 1-28

1.12 Typical Op-Amp Datasheet and Its Specifications:

LM741
Single Operational Amplifier

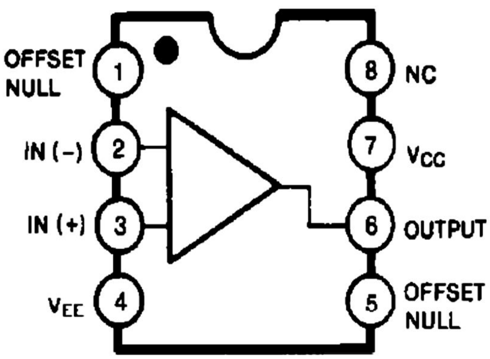
FAIRCHILD
SEMICONDUCTOR®

Features

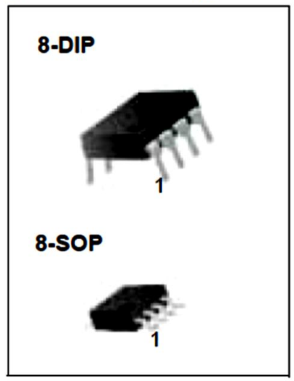
- Short circuit protection
- Excellent temperature stability
- Internal frequency compensation
- High Input voltage range
- Null of offset

Description

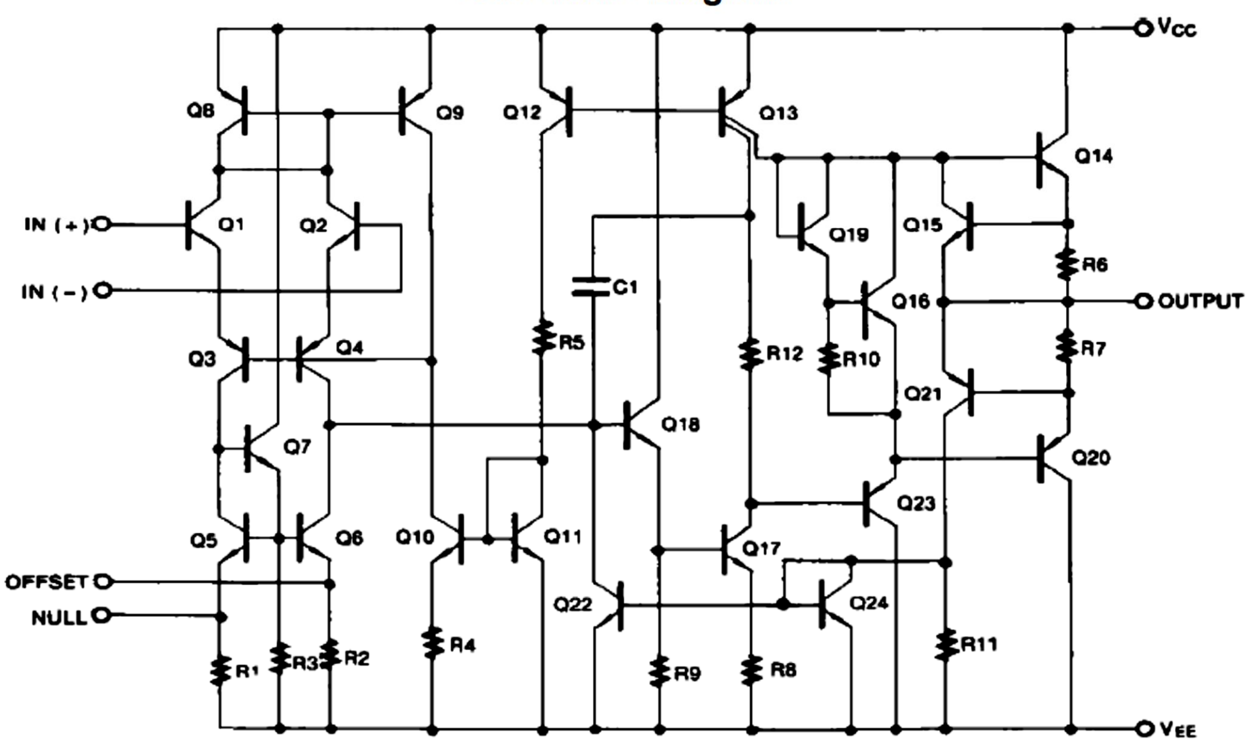
The LM741 series are general purpose operational amplifiers. It is intended for a wide range of analog applications. The high gain and wide range of operating voltage provide superior performance in intergrator, summing amplifier, and general feedback applications.



Internal Block Diagram



Schematic Diagram



Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	LM741	Unit
Supply Voltage	V_{CC}	±18	V
Differential Input Voltage	$V_{I(DIFF)}$	30	V
Input Voltage	V_I	±15	V
Output Short Circuit Duration	-	Indefinite	-
Power Dissipation	P_D	500	mW
Operating Temperature Range	T_{OPR}	0 ~ + 70	°C
Storage Temperature Range	T_{STG}	-65 ~ + 150	°C

Electrical Characteristics

(V_{CC} = 15V, V_{EE} = - 15V. T_A = 25 °C, unless otherwise specified)

Parameter	Symbol	Conditions	LM741 Min.	LM741 Typ.	LM741 Max.	Unit
Input Offset Voltage	V_{IO}	R_S≤10KΩ	-	2.0	6.0	mV
		R_S≤50Ω	-	-	-	
Input Offset Voltage Adjustment Range	$V_{IO(R)}$	V_{CC} = ±20V	-	±15	-	mV
Input Offset Current	I_{IO}	-	-	20	200	nA
Input Bias Current	I_{BIAS}	-	-	80	500	nA
Input Resistance	R_I	V_{CC} =±20V	0.3	2.0	-	MΩ
Input Voltage Range	$V_{I(R)}$	-	±12	±13	-	V
Large Signal Voltage Gain	G_V	R_L≥2KΩ, V_{CC} =±20V, $V_{O(P-P)}$ =±15V	-	-	-	V/mV
		R_L≥2KΩ, V_{CC} =±15V, $V_{O(P-P)}$ =±10V	20	200	-	
Output Short Circuit Current	I_{SC}	-	-	25	-	mA
Output Voltage Swing	$V_{O(P-P)}$	V_{CC} = ±20V, R_L≥10KΩ	-	-	-	V
		V_{CC} = ±20V, R_L≥10KΩ	-	-	-	
		V_{CC} = ±15V, R_L≥10KΩ	±12	±14	-	
		V_{CC} = ±15V, R_L≥10KΩ	±10	±13	-	
Common Mode Rejection Ratio	CMRR	R_S≤10KΩ, V_{CM} = ±12V	70	90	-	dB
		R_S≤50Ω, V_{CM} = ±12V	-	-	-	
Power Supply Rejection Ratio	PSRR	V_{CC} = ±15V to V_{CC} = ±15V, R_S≤50Ω	-	-	-	dB
		V_{CC} = ±15V to V_{CC} = ±15V, R_S≤10KΩ	77	96	-	
Transient Response: Rise Time	t_R	Unity Gain	-	0.3	-	µs
Transient Response: Overshoot	OS	Unity Gain	-	10	-	%
Bandwidth	BW	-	-	-	-	MHz
Slew Rate	SR	Unity Gain	-	0.5	-	V/µs
Supply Current	I_{CC}	R_L= ∞Ω	-	1.5	2.8	mA
Power Consumption	P_C	V_{CC} = ±20V	-	-	-	mW
		V_{CC} = ±15V	-	50	85	

Applications of Operational Amplifiers

2.1 Voltage Summation:

It is possible to scale a signal voltage, that is, to multiply it by a fixed constant, through an appropriate choice of external resistors that determine the closed-loop gain of an amplifier circuit. This operation can be accomplished in either an inverting or noninverting configuration. It is also possible to sum several signal voltages in one operational-amplifier circuit and at the same time scale each by a different factor. This called a linear combination and the circuit that produces it is often called a linear-combination circuit as shown in Fig. 2-1. For the three-input inverting amplifier of Fig. 2-1,

$i_1 + i_2 + i_3 = i_f$ or $\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3} = -\frac{v_o}{R_f}$ =>

$$v_o = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \frac{R_f}{R_3}v_3\right) \qquad [2\text{-}1]$$

when $R_1 = R_2 = R_3 = R$;

$$v_o = -\frac{R_f}{R}(v_1 + v_2 + v_3) \qquad [2\text{-}2]$$

when $R_f = R$;

$$v_o = -(v_1 + v_2 + v_3) \qquad [2\text{-}3]$$

The feedback ratio;

$$\beta = \frac{R_p}{R_p + R_f} \qquad [2\text{-}4]$$

where $R_p = R_1 \| R_2 \| R_3$.

The optimum value of the compensation resistor is

$$R_c = R_f \| R_p = \mathrm{R}_f \| R_1 \| R_2 \| R_3 \qquad [2\text{-}5]$$

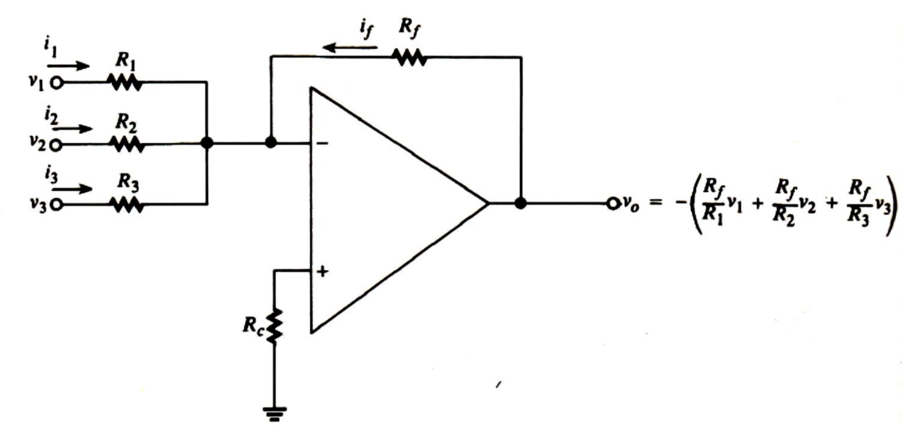


Fig. 2-1

Fig. 2-2 shows a noninverting version of the linear-combination circuit. In this example, only two inputs are connected and it can be shown that

$$v_o = \frac{R_g + R_f}{R_g}\left(\frac{R_2}{R_1 + R_2}v_1 + \frac{R_1}{R_1 + R_2}v_2\right) \qquad [2\text{-}6]$$

Although this circuit does not invert the scaled sum, it is somewhat more cumbersome than the inverting circuit, in applications where a noninverted sum is required, it can be obtained using the inverting circuit of Fig. 2-1, followed by a unity-gain inverter.

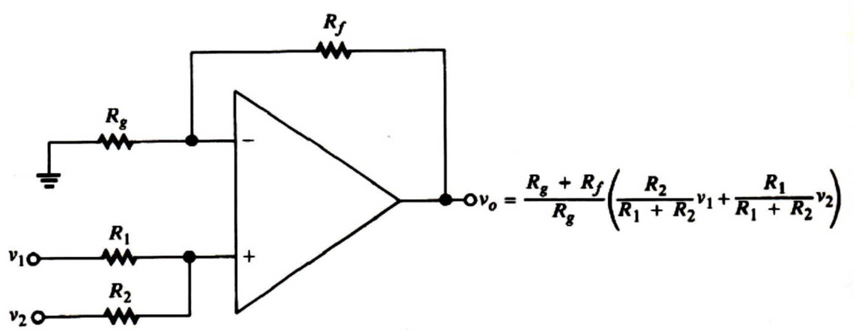


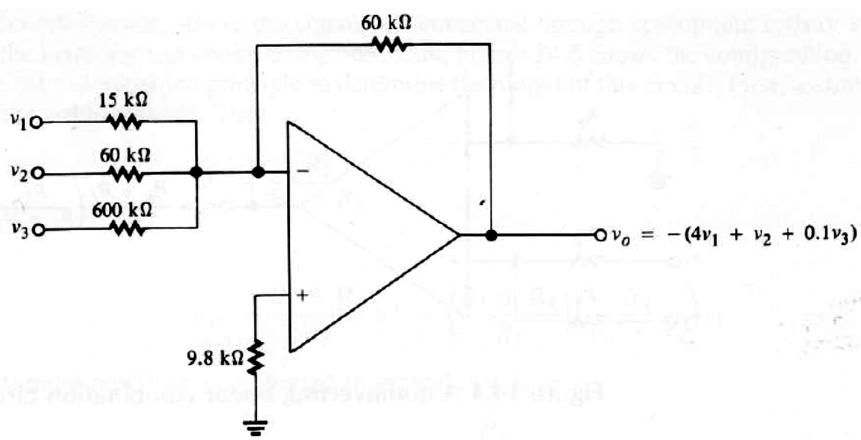
Fig. 2-2

Exercise 2-1:

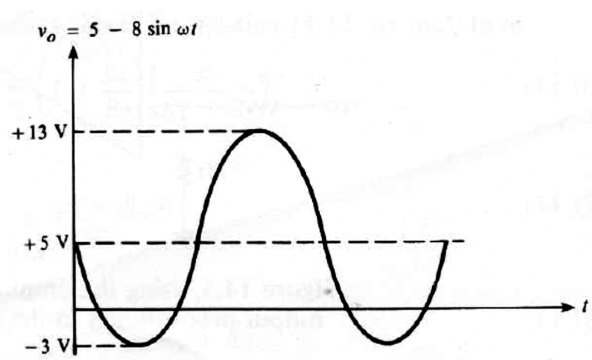
(a) Design an operational-amplifier circuit that will produce an output equal to $-(4v_1 + v_2 + 0.1v_3)$. Use $R_f = 60$ kΩ.

(b) Write an expression for the output and sketch its waveform when $v_1 = 2\,sin\,\omega t$ V, $v_2 = +5$ V dc, and $v_3 = -100$ V dc.

[Answers: (a) $R_1 = 15$ kΩ, $R_2 = 60$ kΩ, $R_3 = 600$ kΩ, $R_c = 9.8$ kΩ, Fig. 2-3(a)
(b) $v_o = 5 - 8\sin\omega t$, Fig. 2-3(b)]



(a)



(b)

Fig. 2-3

2.2 Voltage Subtraction:

Suppose we wish to produce an output voltage that equals the mathematical difference between two input signals. This operation can be performed by using a differential mode, where the signals are connected to the inverting and noninverting terminals. Fig. 2-4 shows the differential configuration. We can use the superposition principle to determine the output of this circuit;

$v^+ = \frac{R_2}{R_1+R_2} v_1$ and $v_{o1} = \frac{R_3+R_4}{R_3} v^+ = \left(\frac{R_3+R_4}{R_3}\right)\left(\frac{R_2}{R_1+R_2}\right) v_1$,

so $v_{o2} = -\frac{R_4}{R_3} v_2$ =>

$$v_o = v_{o1} + v_{o2} = \left(\frac{R_3+R_4}{R_3}\right)\left(\frac{R_2}{R_1+R_2}\right) v_1 - \frac{R_4}{R_3} v_2 \qquad [2\text{-}7]$$

If $R_1 = R_3 = R$ and $R_2 = R_4 = AR$ =>

$v_o = v_{o1} + v_{o2} = \left(\frac{R+AR}{R}\right)\left(\frac{AR}{R+AR}\right) v_1 - \frac{AR}{R} v_2$ =>

$$v_o = A(v_1 - v_2) \qquad [2\text{-}8]$$

where A is a fixed constant, the bias compensation resistance ($R_c = R_1 \| R_2$) is automatically the correct value ($R_3 \| R_4$), namely $R \| AR$.

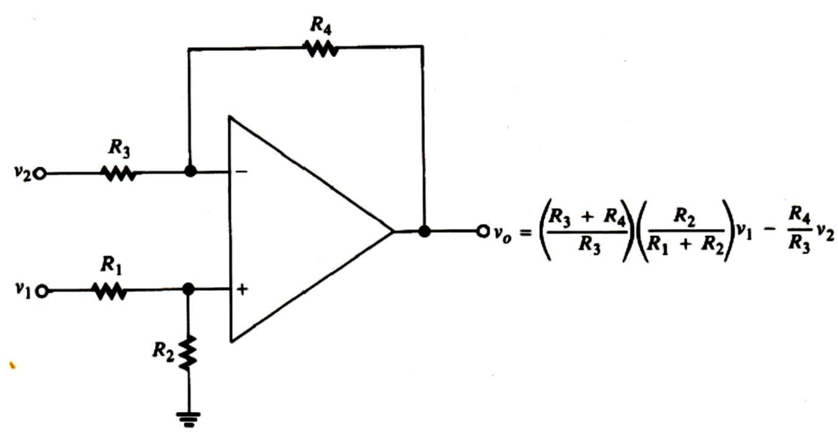


Fig. 2-4

Let the general form of the output of Fig. 2-4 be

$$v_o = a_1 v_1 - a_2 v_2 \qquad [2\text{-}9]$$

where $a_1 = \left(\frac{R_3+R_4}{R_3}\right)\left(\frac{R_2}{R_1+R_2}\right)$ and $a_2 = \frac{R_4}{R_3}$ => $a_1 = (1 + a_2)\left(\frac{R_2}{R_1+R_2}\right)$, but $\frac{R_2}{R_1+R_2} < 1$, to produce $v_o = a_1 v_1 - a_2 v_2$, we must have $a_1 < (1 + a_2)$, this restriction limits the usefulness of the circuit.

Moreover, we note that the compensation resistance ($R_c = R_1 \| R_2$) is not equal to its optimum value $R_3 \| R_4$. With some algebraic complication, we can impose the additional condition $R_1 \| R_2 = R_3 \| R_4$ and thereby force the compensation resistance to have its optimum value. With $v_o = a_1 v_1 - a_2 v_2$, it can be shown that the compensation resistance ($R_c = R_1 \| R_2$) is optimum when the resistor values are selected in accordance with;

$$R_4 = a_1 R_1 = a_2 R_3 = R_2(1 + a_2 - a_1) \qquad [2\text{-}10]$$

Although the circuit of Fig. 2-4 is a useful and economic way to obtain a difference voltage of the form $v_o = A(v_1 - v_2)$, our analysis has shown that it has limitations and complications when we want to produce an output of the general form $v_o = a_1 v_1 - a_2 v_2$. An alternate way to obtain a scaled difference between two signal inputs is to use two inverting amplifiers, as shown in Fig. 2-5.

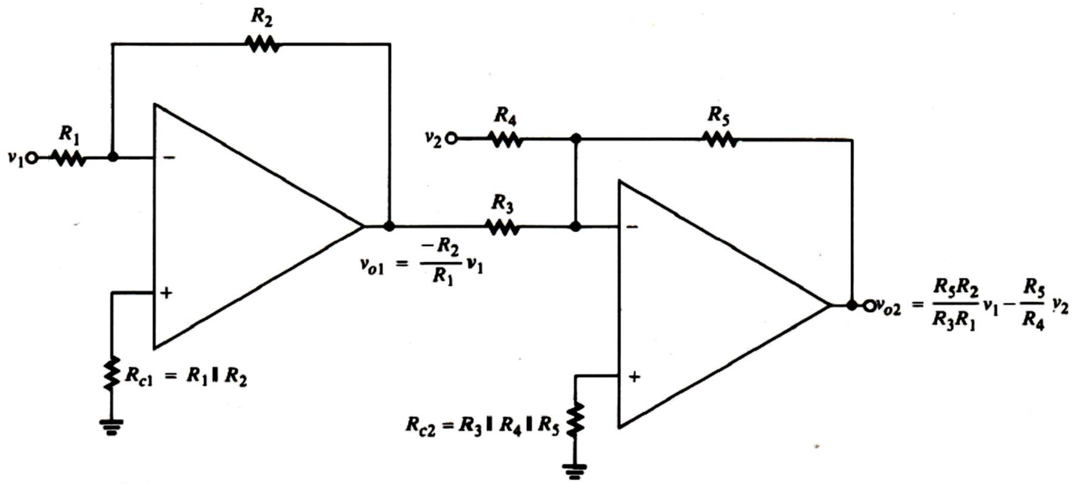


Fig. 2-5

The output of the first amplifier is

$$v_{o1} = -\frac{R_2}{R_1} v_1,$$

and the output of the second amplifier is

$$v_{o2} = -\left(\frac{R_5}{R_3} v_{o1} + \frac{R_5}{R_4} v_2\right) = v_o = \frac{R_5 R_2}{R_3 R_1} v_1 - \frac{R_5}{R_4} v_2 \qquad [2\text{-}11]$$

This equation shows that there is a great deal of flexibility in the choice of resistor values necessary to obtain $v_o = a_1 v_1 - a_2 v_2$, since a large number of combinations will satisfy;

$$a_1 = \frac{R_5 R_2}{R_3 R_1} \text{ and } a_2 = \frac{R_5}{R_4}.$$

Furthermore, there are no restrictions on the choice of values for a_1 and a_2, nor any complications in setting R_c to its optimum value.

Exercise 2-2:

If the resistor values in Fig. 2-4 are chosen in according with
$R_4 = a_1 R_1 = a_2 R_3 = R_2(1 + a_2 - a_1)$, then,
assuming that $a_1 < (1 + a_2)$, show that

(a) $v_o = a_1 v_1 - a_2 v_2$, and
(b) the compensation resistance ($R_c = R_1 \| R_2$) has its optimum value ($R_3 \| R_4$).

Exercise 2-3:

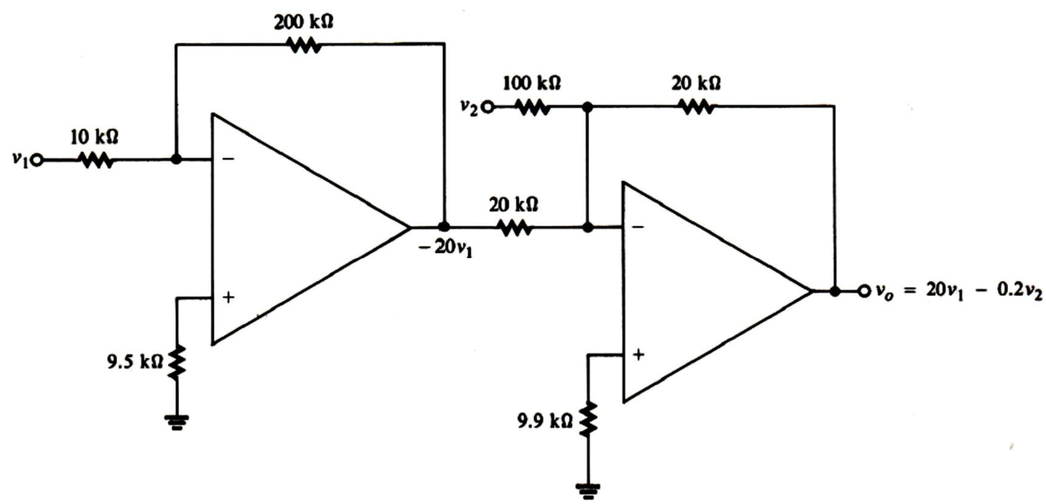
Design an operational-amplifier circuit using the differential configuration to produce the output $v_o = 0.5 v_1 - 2.0 v_2$. Assume $R_4 = 100$ kΩ**.** Check if the compensation resistance has its optimum value.

[Answer: $R_1 = 200$ kΩ, $R_2 = 40$ kΩ, $R_3 = 50$ kΩ, $R_c = 9.8$ kΩ,
$R_c = R_1 \| R_2 = 33.3$ kΩ $= R_3 \| R_4$ (as required)]

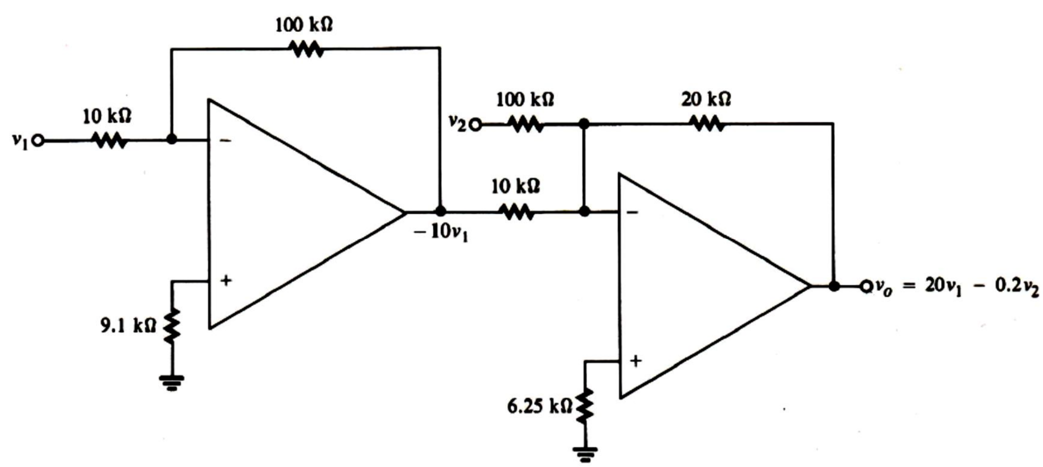
Exercise 2-4:

Design an op-amp circuit to produce the output $v_o = 20v_1 - 0.2v_2$. First, check if you can use the differential circuit.

[Answer: $a_1 = 20 > (1 + a_2) = 1.2$ (we cannot use the differential circuit), Two of many design models are shown in Fig. 2-6(a) and (b)]



(a)



(b)

Fig. 2-6

Exercise 2-5:

(a) Design an operational-amplifier circuit using two inverting configurations to produce the output $v_o = -10v_1 + 5v_2 + 0.5v_3 - 20v_4$. Choose feedback resistor $R_f = 100\ \text{k}\Omega$ for each amplifier.

(b) Assuming that the unity-gain frequency of each amplifier is 1 MHz, find the approximate, overall, closed-loop bandwidth of your solution.

[Answers: (a) One of many possible solutions is shown in Fig. 2-7, (b) $BW_{CL(Overall)}$ = Min. (BW_{CL1}= 153.8 kHz, BW_{CL2}= 31.2 kHz) = 31.2 kHz]

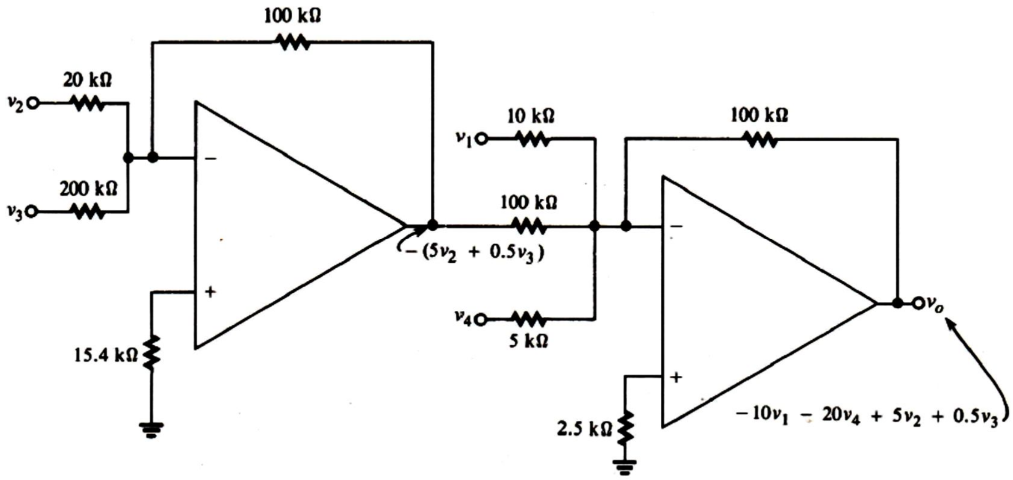


Fig. 2-7

2.3 Controlled Voltage and Current Sources:

A ***controlled*** source is one whose output voltage or current is determined by magnitude of another, independent voltage or current.

2.3.1 Voltage-Controlled Voltage Source (VCVS):

An ideal, voltage-controlled voltage source is one whose output voltage V_o equals a fixed constant (k) times the value of another, controlling voltage: $V_o = kV_i$; and is independent of the current drawn from it. The constant k is dimensionless. Both the inverting and noninverting configurations of an ideal operational amplifier meet the two criteria. In each case, the output voltage equals a fixed constant (the closed-loop gain, determined by external resistors) times an input voltage. Also, since the output resistance is (ideally) 0, there is no voltage division at the output and the voltage is independent of load.

2.3.2 Voltage-Controlled Current Source (VCCS):

An ideal, voltage-controlled current source is one that supplies a current whose magnitude equals a fixed constant (k) times the value of an independent controlling voltage: $I_o = kV_i$; and is independent of the load to which the current is supplied. The constant k has the dimensions of conductance (siemens). Since it relates output current to input voltage, it is called the ***transconductance***, g_m, of the source. Fig. 2-8 shows two familiar amplifier circuits: the inverting and noninverting configurations of an op-amp.

In Fig. 2-8(a), v^- is virtual ground, so $I_1 = V_{in}/R_1$. Since no current flows into the inverting terminal of the ideal amplifier, $I_L = I_1$, or

$$I_L = V_{in}/R_1 = g_m V_{in} \qquad [2\text{-}12]$$

The transconductance $g_m = 1/R_1$ siemens. Since R_L does not appear in the equation, so the load current is independent of load resistance. This version of a controlled current source is said to have a ***floating load***, because neither side of R_L can be grounded.

In Fig. 2.8(b), $v^- = V_{in}$, so $I_1 = V_{in}/R_1$. Once again, no current flows into the inverting terminal, so $I_L = I_1$. Therefore, $I_L = V_{in}/R_1 = g_m V_{in}$. As in the inverting configuration, the load current is independent of R_L and the transconductance is $1/R_1$ siemens. The load is also floating in this version.

Of course, there is a practical limit on the range of load resistance R_L that can be used in each circuit. If R_L, is made too large, the output voltage of the amplifier will approach its maximum limit, as determined by the power supply voltages. For successful operation, the load resistance in each circuit must obey

$$R_L < \frac{R_1|V_{max}|}{V_{in}} \quad \text{(inverting circuit)}$$

$$R_L < R_1\left(\frac{|V_{max}|}{V_{in}} - 1\right) \quad \text{(noninverting circuit)} \qquad [2\text{-}13]$$

where $|V_{max}|$ is the magnitude of the maximum output voltage of the amplifier.

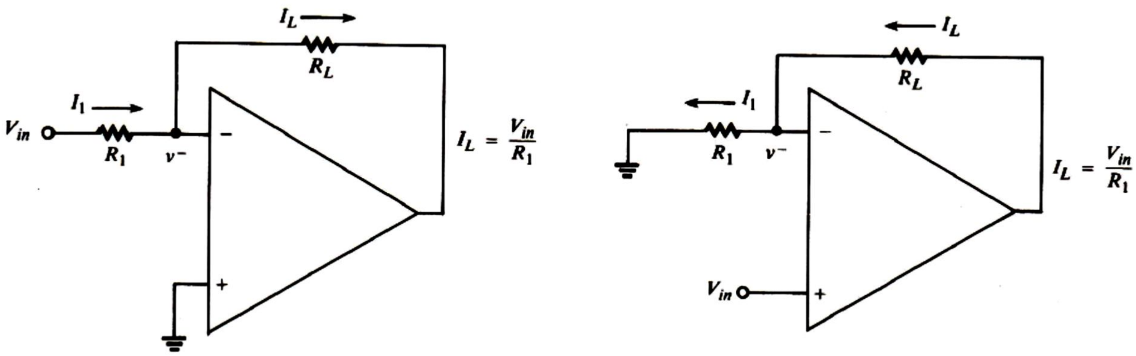


Fig. 2-8

Fig. 2-9 shows a voltage-controlled current source that can be operated with a grounded load. Since there is (ideally) zero current into the + input, Kirchhoff's current law at the node where R_L is connected to the + input gives

$$V_L = v^+ = v^- = \frac{RV_o}{R+R} = \frac{V_o}{2} \quad \text{and}$$

$$I_L = I_1 + I_2 = \frac{V_{in}-V_L}{R} + \frac{V_o-V_L}{R} = \frac{V_{in}}{R} - \frac{V_o}{2R} + \frac{V_o}{R} - \frac{V_o}{2R} \Rightarrow$$

$$I_L = V_{in}/R = g_m V_{in} \qquad [2\text{-}14]$$

This equation shows that the load current is controlled by V_{in}, and that it is independent of R_L. For successful operation, the load resistance must obey

$$R_L < \frac{R|V_{max}|}{2V_{in}} \qquad [2\text{-}15]$$

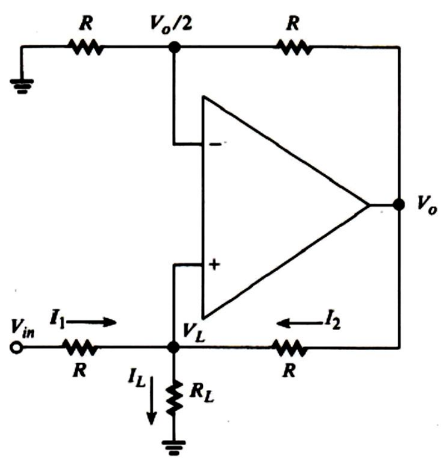


Fig. 2-9

Exercise 2-6:

Design an inverting, floating load, voltage-controlled current source that will supply a constant current of 0.2 mA when the controlling voltage is 1 V. What is the maximum load resistance for this supply if the maximum amplifier output voltage is 20 V?

[Answer: $R_1 = 1/g_m = 5\ \text{k}\Omega$, $R_L < 100\ \text{k}\Omega$, Fig. 2-10]

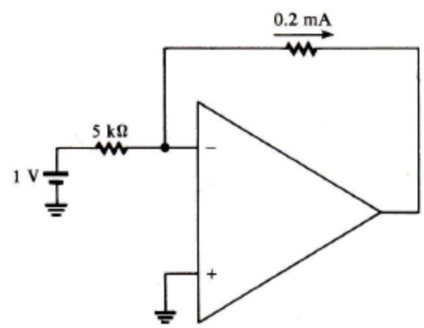


Fig. 2-10

Exercise 2-7:

Find the current through each resistor and the voltage at each node of the voltage-controlled current source in Fig. 2-11. What is the transconductance of the source?

[Answer: $V_A = 3.75$ V, $V_B = 7.5$ V, $V_C = 3.75$ V, $I_L = 2.5$ mA, $I_1 = 1.5625$ mA, $I_2 = 0.9375$ mA, $I_3 = 0.9375$ mA, $I_4 = 0.9375$ mA, $g_m = 0.25$ nS]

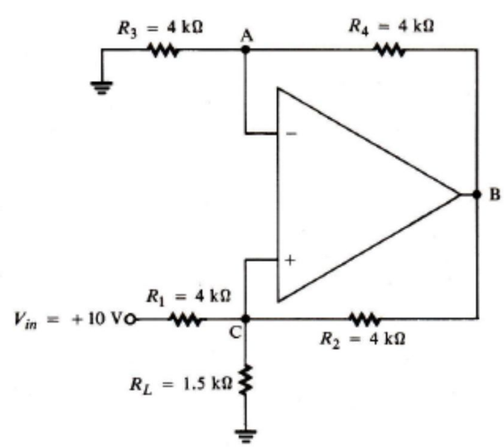


Fig. 2-11

2.3.3 Current-Controlled Voltage Source (CCVS):

An ideal current-controlled voltage source has an output voltage that is equal to a constant (k) times the magnitude of an independent current: $v_o = kI_i$; and is independent of the load connected to it. Here, the constant k has the units of ohms. A current controlled voltage source can be thought of as a ***current-to-voltage converter***, since output voltage is proportional to input current. It is useful in applications where current measurements are required, because it is generally more convenient to measure voltages.

Fig. 2-12 shows a very simple current-controlled voltage source. Since no current flows into the − input, the controlling current I_{in}, is the same as the current in feedback resistor R. Since v^- is virtual ground,

$$V_o = -I_{in}R \qquad [2\text{-}16]$$

Once again, the fact that the amplifier has zero output resistance implies that the output voltage will be independent of load.

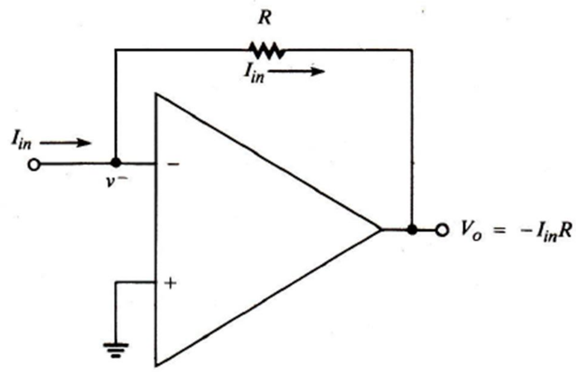


Fig. 2-12

2.3.4 Current-Controlled Current Source (CCCS):

An ideal current-controlled current source is one that supplies a current whose magnitude equals a fixed constant (k) times the values of an independent controlling current: $I_o = kI_i$; and is independent of the load to which the current is supplied. The constant k is dimensionless, since it is the ratio of two currents.

Fig. 2-13 shows a current-controlled current source with floating load R_L. Since no current flows into the − input, the current in R_2 must equal I_{in}. Since v^- is at virtual ground,

$$V_2 = -I_{in}R_2 \;\Rightarrow\; I_1 = \frac{0 - V_2}{R_1} = \frac{I_{in}R_2}{R_1} \text{ and } I_L = I_1 + I_{in} = \frac{R_2}{R_1}I_{in} + I_{in} \;\Rightarrow$$

$$I_L = \left(\frac{R_2}{R_1} + 1\right) I_{in} \qquad [2\text{-}17]$$

This equation shows that the load current equals the constant ($1 + R_2/R_1$) times the controlling current and that I_L is independent of R_L. For successful operation, R_L must obey

$$R_L < \left(\frac{|V_{max}|}{I_{in}} - R_2\right)\left(\frac{R_1}{R_1 + R_2}\right) \qquad [2\text{-}18]$$

The circuit of Fig. 2.13 may be regarded as a current amplifier, the amplification factor being

$$k = I_L/I_{in} = 1 + R_2/R_1 \qquad [2\text{-}19]$$

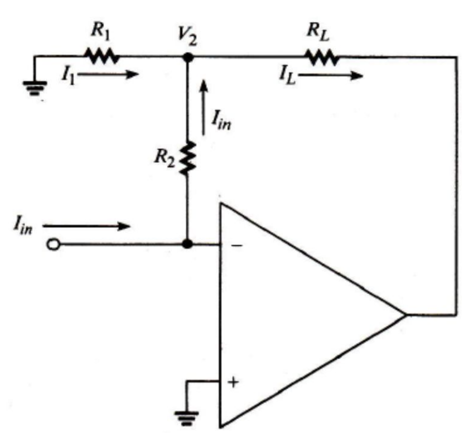


Fig. 2-13

Exercise 2-8:

It is desired to measure a dc current that ranges from 0 to 1 mA using an ammeter whose most sensitive range is 0 to 10 mA. To improve the measurement accuracy, the current to be measured should be amplified by a factor of 10.

(a) Design the circuit.

(b) Assuming that the meter resistance is 150 Ω and the maximum output voltage of the amplifier is 15 V, verify that the circuit will perform properly.

[Answers: (a) Fig. 2-14, $k = I_L/I_X = 1 + R_2/R_1 = 10$ as required,
(b) $R_{meter} = 150\ \Omega < R_L = 600\ \Omega$]

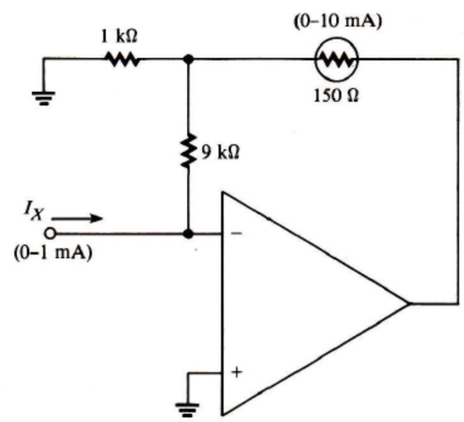


Fig. 2-14

2.4 Op-Amp Integrators:

An electronic integrator is a device that produces an output waveform whose value at any instant of time equals the total area under the input waveform up to that point in time. A mathematical integration, the process produces the time varying function $\int_0^t v_{in} dt$. To illustrate this concept, suppose the input to an electronic integrator is the dc level E volts, which is first connected to integrator at an instant of time we will call $t = 0$. Refer to Fig. 2-15. The plot of the dc "waveform" versus time is simply a horizontal line at level E volts, since the dc voltage is constant. The more time that we allow to pass, the greater the area that accumulates under the dc waveform. At any time-point t, the total area under the input waveform between time 0 and time t is (height) × (width) = Et, volts, as illustrated in figure. For example, if $E = 5$ V dc, then the output will be 5 V at $t = 1$ s, 10 V at $t = 2$ s, 15 V at $t = 3$ s, and so forth. We see that the output is the ramp voltage $v(t) = Et$.

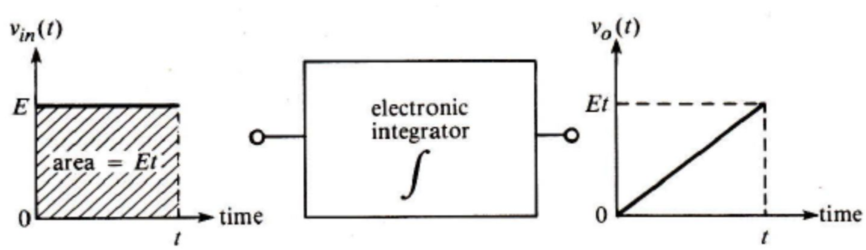


Fig. 2-15

Fig. 2-16 shows how an electronic integrator is constructed using an operational amplifier. The component in the feedback path is capacitor C, and the amplifier is operated in an inverting configuration. To represent integration of the voltage v between time 0 and time t, we are assuming zero input offset, the output of this circuit is

$$v_o(t) = \frac{-1}{R_1 C}\int_0^t v_{in} dt \qquad [2\text{-}20]$$

This equation shows that the output is the (inverted) integral of the input, multiplied by the constant $1/R_1C$. If this circuit were used to integrate the dc waveform shown in Fig. 2-15, the output would be a negative-going ramp ($v_o = -Et/R_1C$).

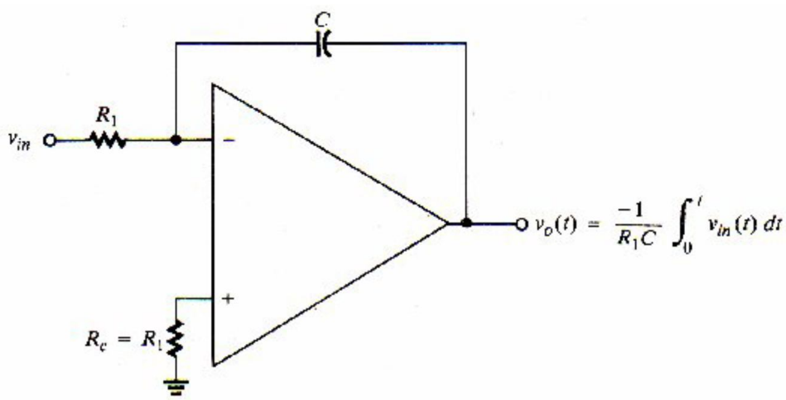


Fig. 2-16

Now we demonstrate why the circuit of Fig. 2-16 performs integration. Since the current into the − input is 0, we have, from Kirchhoff's current law;

$$i_1 + i_C = 0,$$

where i_1 is the input current through R_1 and i_C is the feedback current through the capacitor. Since $v^- = 0$, the current in the capacitor is

$$i_C = C\frac{dv_o}{dt} \;\Rightarrow\; \frac{v_{in}}{R_1} + C\frac{dv_o}{dt} = 0 \quad \text{or} \quad \frac{dv_o}{dt} = \frac{-1}{R_1\,C}v_{in}.$$

Integrating both sides of the last equation with respect to t, we obtain

$$v_o(t) = \frac{-1}{R_1 C}\int_0^t v_{in} dt.$$

It can be shown, using calculus, that the mathematical integral of the sine wave $A \sin \omega t$ is

$$\int (A \sin \omega t)\, dt = \frac{-A}{\omega}\sin(\omega t + 90) = \frac{-A}{\omega}\cos(\omega t).$$

Therefore, if the input to the inverting integrator in Fig. 2-16 is $v_{in} = A \sin \omega t$, the output is

$$v_o = \frac{-1}{R_1 C}\int (A \sin \omega t)\, dt = \frac{-A}{\omega R_1 C}(-\cos \omega t) = \frac{A}{\omega R_1 C}\cos \omega t \qquad [2\text{-}21]$$

The most important fact revealed by Eqn. [2-21] is that the output of an integrator with sinusoidal input is a sinusoidal waveform whose amplitude is inversely proportional to its frequency. This observation follows from the presence of ω (= $2\pi f$) in the denominator of Eqn. [2-21].

A gain magnitude is the ratio of the peak value of the output to the peak value of the input:

$$\left|\frac{v_o}{v_{in}}\right| = \frac{A}{A\omega R_1 C} = \frac{1}{\omega R_1 C} \qquad [2\text{-}22]$$

This equation clearly shows that gain is inversely proportional to frequency.

Although high-quality, precision integrators are constructed as shown in Fig. 2-16 for use in low-frequency applications such as analog computers, these applications require high-quality amplifiers with extremely small offset voltages. As mentioned earlier, any input offset is integrated as if it were a dc signal input and will eventually cause the amplifier to saturate. To eliminate this problem in ***practical integrators*** using general purpose amplifiers, a resistor is connected in parallel with the feedback capacitor, as shown in Fig. 2-17. Since the capacitor is an open circuit as dc is concerned, the dc closed-loop gain of the integrator is $-R_f/R_1$. At high frequencies, X_C is much smaller than R_f, so the parallel combination of C and R_f is essentially the same as C alone, and signals are integrated as usual.

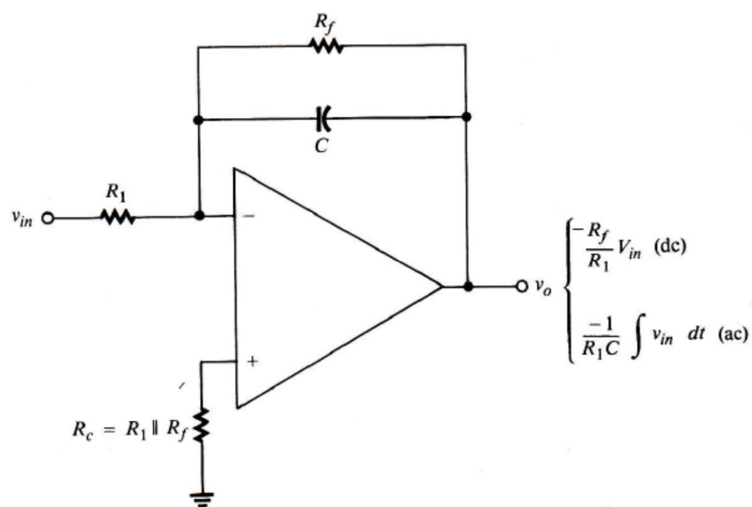


Fig. 2-17

While the feedback resistor in Fig. 2-17 prevents integration of dc inputs, it also degrades the integration of low-frequency signals. At frequencies where the capacitive reactance of C is comparable in value to R_f, the net feedback impedance is not predominantly capacitive and true integration does not occur. As a rule, we can say that satisfactory integration will occur at frequencies much greater than the frequency at which $X_C = R_f$. That is, for integrator action we want

$$X_C << R_f \Rightarrow \frac{1}{2\pi f C} << R_f \Rightarrow$$

$$f >> \frac{1}{2\pi R_f C} \qquad [2\text{-}23]$$

The frequency f_c where $X_C = R_f$,

$$f_c = \frac{1}{2\pi R_f C} \qquad [2\text{-}24]$$

Eqn. [2-24] defines a break frequency, f_c, in the Bode plot of the practical integrator. As shown in Fig. 2-18, at frequencies well above f_c, the gain falls off at the rate of −20 dB/decade, like that of an ideal integrator, and at frequencies below f_c, the gain approaches its dc value of R_f/R_1. Because the integrator's output amplitude or gain decreases with frequency, it is a kind of low-pass filter.

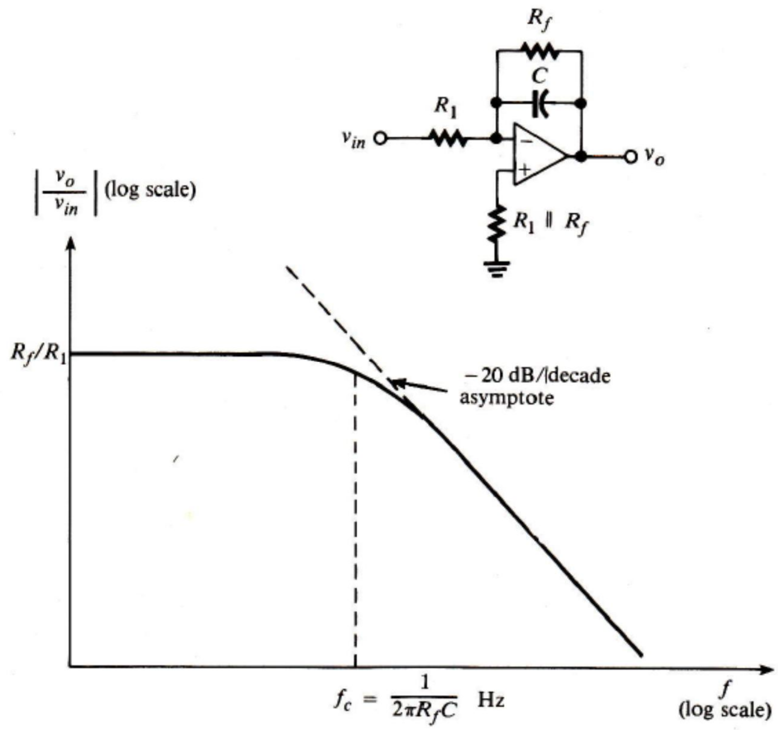


Fig. 2-18

In closing our discussion of integrators, we should note that it is possible to scale and integrate several input signals simultaneously, using an arrangement similar to the linear combination circuit studied earlier. Fig. 2-19 shows a practical, three-input integrator that performs the following operation at frequencies above f_c:

$$v_o = -\int \left(\frac{1}{R_1 C} v_1 + \frac{1}{R_2 C} v_2 + \frac{1}{R_3 C} v_3\right) dt$$

$$v_o = -\frac{1}{R_1 C}\int v_1 dt - \frac{1}{R_2 C}\int v_2 dt - \frac{1}{R_3 C}\int v_3 dt \qquad [2\text{-}25]$$

If $R_1 = R_2 = R_3 = R$, then

$$v_o = \frac{-1}{RC}\int (v_1 + v_2 + v_3) dt \qquad [2\text{-}26]$$

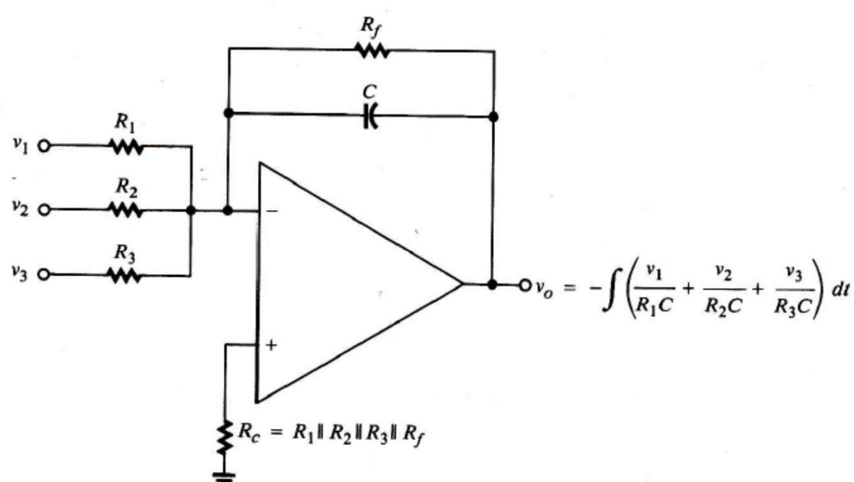


Fig. 2-19

Exercise 2-9:

(a) Find the peak value of the output of the ideal integrator shown in Fig. 2-20. The input is $v_{in} = 0.5 \sin(100t)$ V.

(b) Repeat, when $v_{in} = 0.5 \sin(10^3 t)$ V.

[Answers: (a) $v_o = 5 \cos(100t)$ V => peak value = 5 V,
(b) $v_o = 0.5 \cos(1000t)$ V => peak value = 0.5 V]

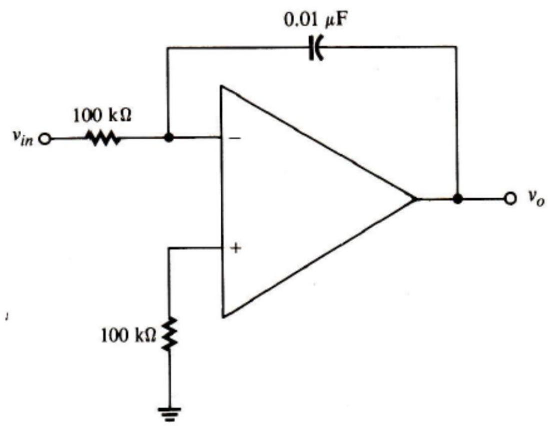


Fig. 2-20

Exercise 2-10:

Design a practical integrator that

(a) integrates signals with frequencies down to 100 Hz, and

(b) produces a peak output of 0.1 V when v_{in} is a 10 V peak sine wave at frequency 10 kHz. Choose $C = 0.01$ μF.

Find the dc component in the output when there is a +50 mV dc input.

[Answer: $R_f = 1.59$ MΩ, $R_1 = 159$ kΩ, $R_c = 145$ kΩ, $v_o = -0.5$ V, Fig. 2-21]

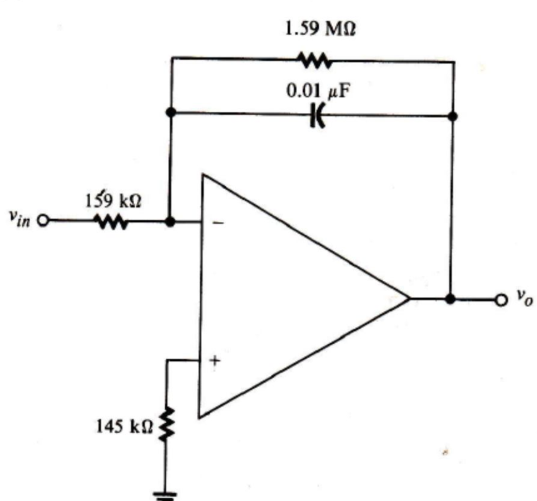


Fig. 2-21

2.5 Op-Amp differentiators:

An electronic differentiator produces an output waveform whose value at any instant of time is equal to the rate of change of the input at that point in time. Fig. 2-22 demonstrates the operation of an ideal electronic differentiator. The input is the ramp voltage $v_{in} = Et$. The rate of change, or slope, of this ramp is a constant E volts/second. Since the rate of change of the input is constant, we see that the output of the differentiator is the constant dc level E volts. We would write

$$\frac{dv_{in}}{dt} = \frac{d(Et)}{dt} = E \qquad [2\text{-}27]$$

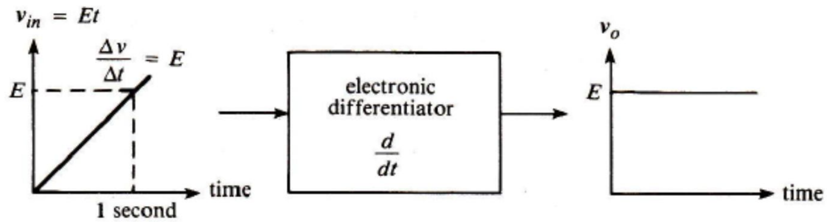


Fig. 2-22

Fig. 2-23 shows how an ideal differentiator is constructed using an operational amplifier. Note that we now have a capacitive input and a resistive feedback-again, just the opposite of an integrator. It can be shown that the output of this differentiator is

$$v_o = -R_f C \frac{dv_{in}}{dt} \qquad [2\text{-}28]$$

Now, we can show how the circuit of Fig. 2-23 performs differentiation. Since the current into the − terminal is 0, we have, from Kirchhoff's current law, $i_C + i_f = 0$.

Since $v^- = 0$, $v_C = v_{in}$ and $i_C = C\frac{dv_{in}}{dt}$.

Also, $i_f = \frac{v_o}{R_f}$, so $C\frac{dv_{in}}{dt} + \frac{v_o}{R_f} = 0$ or $v_o = -R_f C\frac{dv_{in}}{dt}$.

If the input to the inverting integrator in Fig. 2- 23 is $v_{in} = A \sin \omega t$, the output is

$$v_o = -R_f C \frac{d(A\sin\omega t)}{dt} = -A\omega R_f C\cos(\omega t) = A\omega R_f C\sin(\omega t - 90^\circ) \qquad [2\text{-}29]$$

Eqn. [2-29] shows that when the input is sinusoidal, the amplitude of the output of a differentiator is directly proportional to frequency. Also the output lags the input by 90°, regardless of frequency. The gain of the differentiator is

$$\left|\frac{v_o}{v_{in}}\right| = \frac{A\omega R_f C}{A} = \omega R_f C \qquad [2\text{-}30]$$

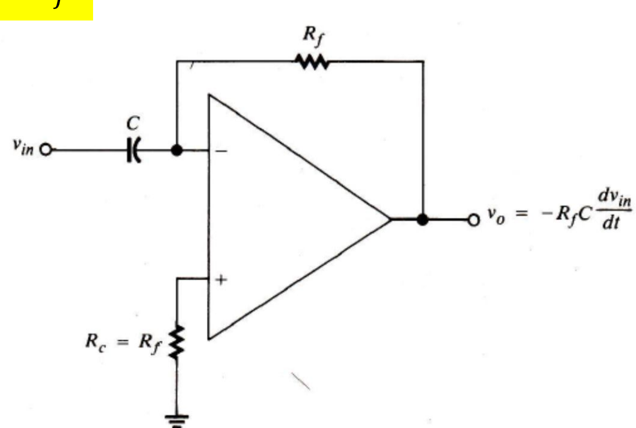


Fig. 2-23

In a ***practical differentiator***, the amplification of signals in direct proportion to their frequencies cannot continue indefinitely as frequency increases, because the amplifier has a finite bandwidth. As we have already known, there is some frequency at which the output amplitude must begin to fall off. Nevertheless, it is often desirable to design a practical differentiator so that it will have a break frequency even lower than that determined by the upper cutoff frequency of the amplifier, that is, to roll off its gain characteristic at some relatively low frequency. This action is accomplished in a practical differentiator by connecting a resistor in series with the input capacitor, as shown in Fig. 2-24. We can understand how this modification achieves the stated goal by considering the net impedance of the R_1C combination at low and high frequencies:

$$Z_{in} = R_1 - j/\omega C \;\; =>$$

$$|Z_{in}| = \sqrt{R_1^2 + (1/\omega C)^2}\;.$$

At very small values of ω, Z_{in}, is dominated by the capacitive reactance component, so the combination is essentially the same as C alone, and differentiator action occurs. At very high values of ω, $1/\omega C$ is negligible, so Z_{in} is essentially the resistance R_1, and the circuit behaves like an ordinary inverting amplifier.

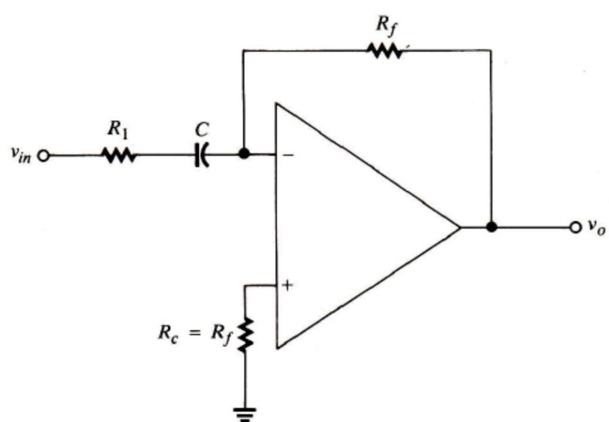


Fig. 2-24

The break frequency f_b beyond which differentiation no longer occurs in Fig. 2-24 is the frequency at which $X_C = R_1$:

$$X_C = \frac{1}{2\pi f_b C} = R_1 \;\; => \;\; f_b = \frac{1}{2\pi R_1 C} \qquad [2\text{-}31]$$

In designing a practical differentiator, the break frequency should be set well above the highest frequency at which accurate differentiation is desired:

$$f_b >> f_h \qquad [2\text{-}32]$$

where f_h is the highest differentiation frequency. Fig. 2-25 shows Bode plots for the gain of the ideal and practical differentiators. In the low-frequency region where differentiation occurs, note that the gain rises with frequency at the rate of 20 dB/decade. The plot shows that the gain levels off beyond the break frequency f_b and then falls off at −20 dB/decade beyond the amplifier's upper cutoff frequency. Recall that the closed-loop bandwidth, or upper cutoff frequency of the amplifier, is given by

$$f_2 = \beta f_t \qquad [2\text{-}33]$$

where β in this case is $R_1/(R_1 + R_f)$.

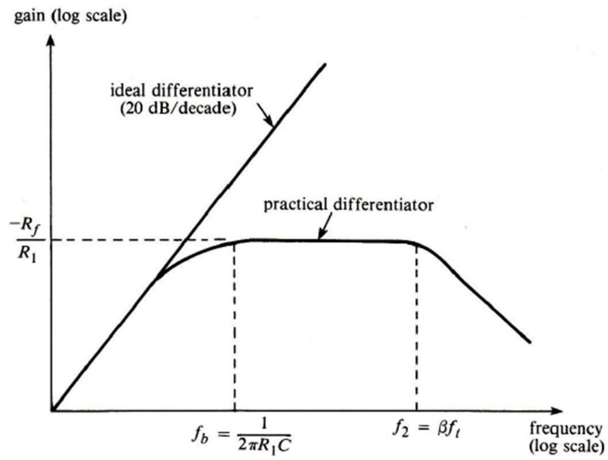


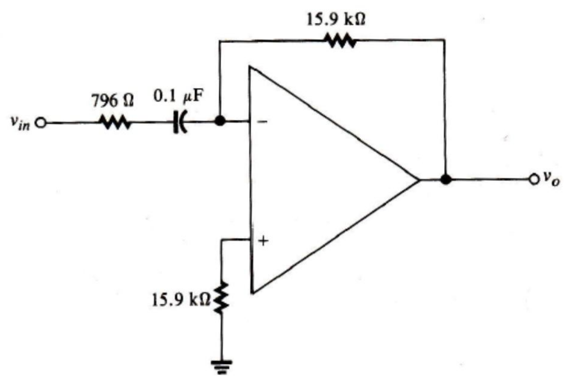
Fig. 2-25

Exercise 2-11:

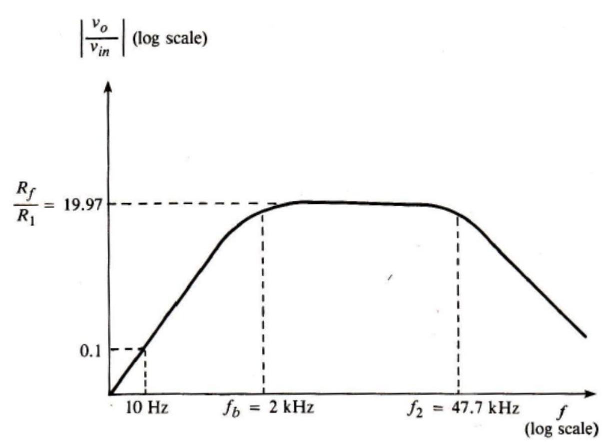
(a) Design a practical differentiator that will differentiate signals with frequencies up to 200 Hz. The gain at 10 Hz should be 0.1. Choose $f_b = 10\, f_h$, and $C = 0.1$ µF.

(b) If the operational amplifier used in the design has a unity-gain frequency of 1 MHz, what is the upper cutoff frequency of the differentiator?

[Answer: (a) $R_1 = 796\ \Omega$, $R_f = 15.9\ \text{k}\Omega$, Fig. 2-26(a)
(b) $f_2 = 47.7$ kHz, Fig. 2-26(b)]



(a)



(b)

Fig. 2-26

2.6 Instrumentation Amplifiers:

An amplifier can be operated in a differential mode to produce an output voltage proportional to the difference between two input signals. Differential operation is a common requirement in instrumentation systems and other signal-processing applications where high accuracy is important. Fig 2-27 shows an improved configuration for producing an output proportional to the difference between two inputs. Notice that the circuit is basically the difference amplifier discussed earlier, with the addition of two input stages. Each input signal is connected directly to the noninverting terminal of an operational amplifier, so each signal source sees a very large input resistance. This circuit arrangement is so commonly used that it is called an ***instrumentation amplifier*** and is commercially available by that name in single-package units. These devices use closely matched, high-quality amplifiers and have very large common-mode rejection ratios.

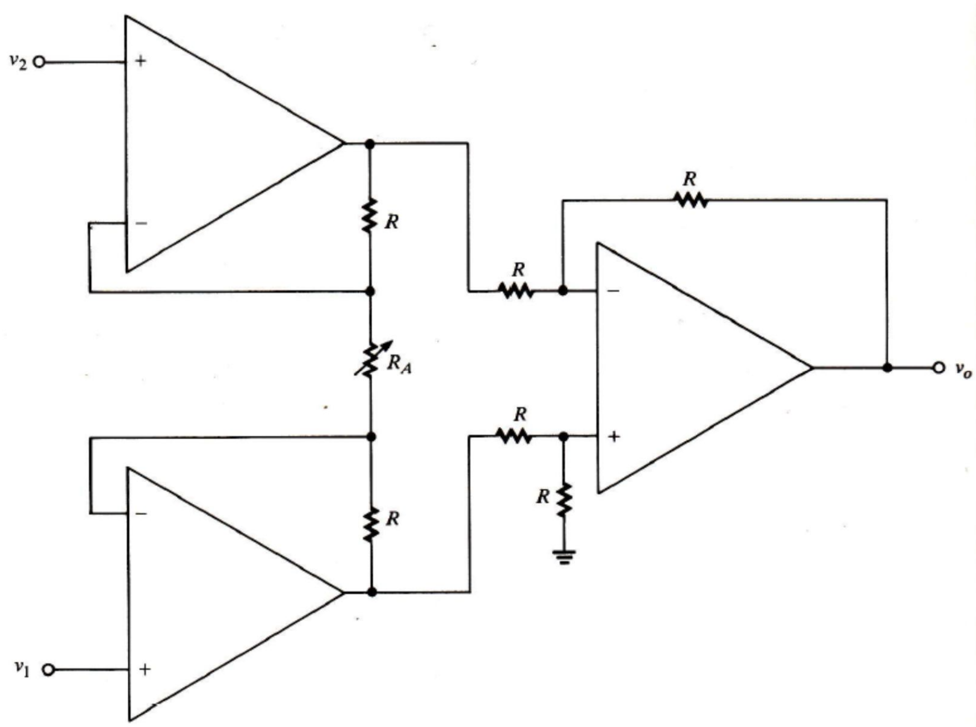


Fig. 2-27

In our analysis of the instrumentation amplifier, we will refer to Fig. 2.28, which shows current and voltage relations in the circuit. we begin by noting that the usual assumption of ideal amplifiers allows us to equate v_i^+ and v_i^- at each input amplifier ($v_i^+ - v_i^- \approx 0$), with the result that input voltages v_1 and v_2 appear across adjustable resistor R_A in Fig. 2-28. For analysis purposes, let us assume that $v_1 > v_2$. Then, the current i through R_A is

$$i = \frac{v_1 - v_2}{R_A}.$$

Since no current flows into either amplifier input terminal, the current i must also flow in each resistor R connected on opposite sides of R_A. Therefore, the voltage drop across each of those resistors is

$$v_R = iR = \frac{(v_1 - v_2)R}{R_A} \qquad [2\text{-}34]$$

The output voltages v_{o1} and v_{o2} are given by

$$v_{o1} = v_1 + v_R$$
$$v_{o2} = v_2 - v_R \qquad [2\text{-}35]$$

Voltages v_{o1} and v_{o2} are the input voltages to the differential stage. Since the external resistors connected to that stage are all equal to R, we recall (with A = 1) that

$$v_o = v_{o1} - v_{o2}$$
$$v_o = (v_1 + v_R) - (v_2 - v_R) = v_1 - v_2 + 2v_R$$
$$v_o = v_1 - v_2 + \frac{2(v_1 - v_2)R}{R_A} \quad =>$$
$$v_o = (v_1 - v_2)\left(1 + \frac{2R}{R_A}\right) \qquad [2\text{-}36]$$

Eqn. 2-36 shows that the output of the instrumentation amplifier is directly proportional to the difference voltage (v_1 and v_2), as required. The overall closed-loop gain is

$$\frac{v_o}{v_1 - v_2} = 1 + \frac{2R}{R_A} \qquad [2\text{-}37]$$

R_A is made adjustable so that gain can be easily adjusted for calibration purposes. Note that the gain is inversely proportional to R_A.

To ensure proper operation of the instrumentation amplifier, all three of the following inequalities must be satisfied at all times:

$$\left|\left(1 + \frac{R}{R_A}\right)v_1 - \frac{R}{R_A}v_2\right| < \left|V_{\max(1)}\right| \qquad [2\text{-}38]$$
$$\left|\left(1 + \frac{R}{R_A}\right)v_2 - \frac{R}{R_A}v_1\right| < \left|V_{\max(1)}\right| \qquad [2\text{-}39]$$
$$\left(1 + \frac{2R}{R_A}\right)\left|v_1 - v_2\right| < \left|V_{\max(2)}\right| \qquad [2\text{-}40]$$

where $V_{\max(1)}$ is the maximum output voltage of each input stage and $V_{\max(2)}$ is the maximum output voltage of the differential (output) stage.

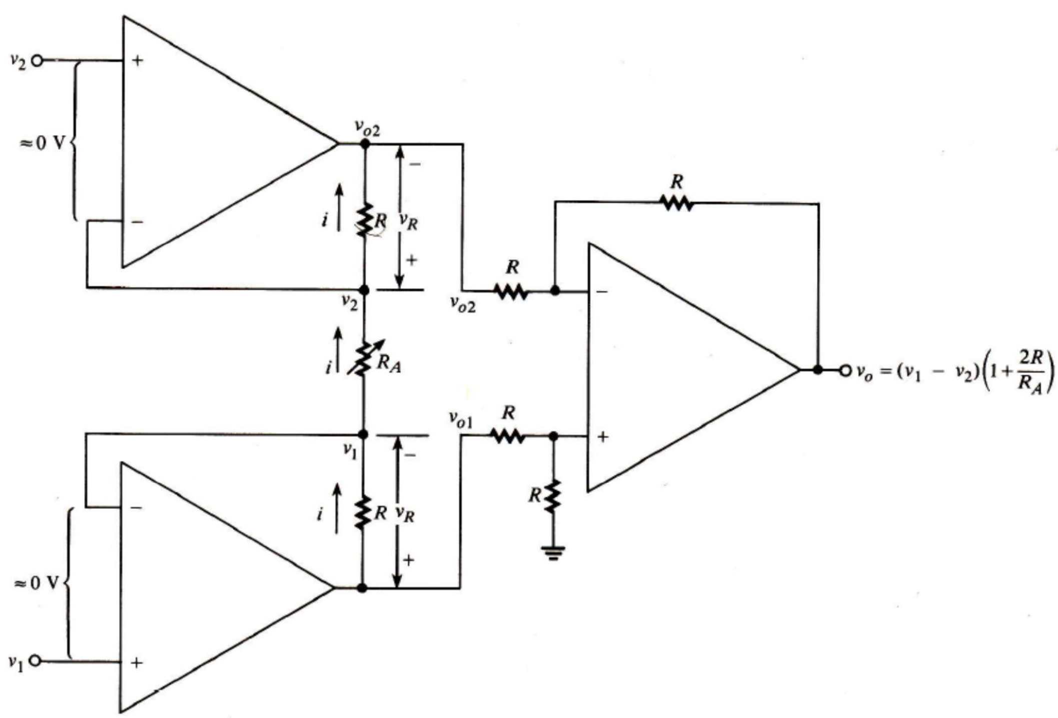


Fig. 2-28

Exercise 2-12:

(a) Assuming ideal amplifiers, find the minimum and maximum output voltage V_o, that is, V_o(min) and V_o(max), of the instrumentation amplifier shown in Fig. 2-29 when the l0 kΩ potentiometer R_p is adjusted through its entire range.

(b) Find V_{o1} and V_{o2} when R_p is set in the middle of its resistance range.

[Answers: (a) $V_o(\text{min}) = 1.45$ V, $V_o(\text{max}) = 20.5$ V,
(b) $V_{o1} = 1.209$ V, $V_{o2} = -1.109$ V]

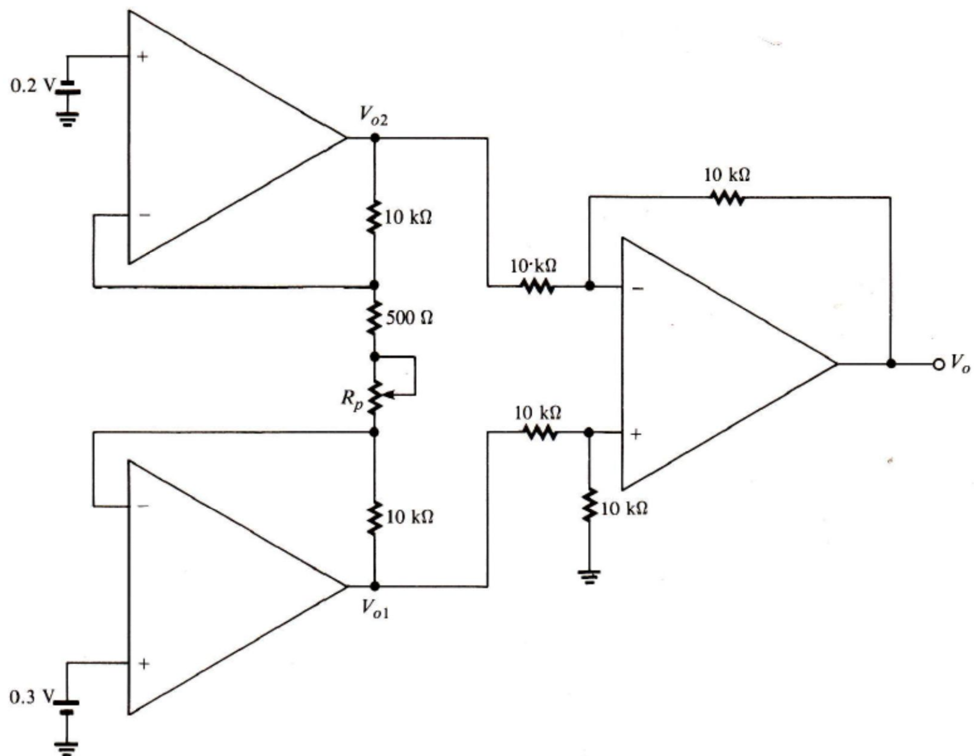


Fig. 2-29

Exercise 2-13:

The maximum output voltages for all three operational amplifiers in an instrumentation amplifier are +15 V. For a particular application, it is known that input signal v_1 may vary from 0 V to 0.8 V and input signal v_2 from 0 V to 1.3 V. Assuming that $R = 2$ kΩ, design the circuit for maximum possible closed-loop gain.

[Answer: $R_A > 112.68$ Ω, $R_A > 173.30$ Ω, $R_A > 189.71$ Ω,
$R_A > 106.67$ Ω, $R_A > 379.56$ Ω, $R_A > 225.35$ Ω,
$R_A(\text{max}) \approx 390$ Ω (standard/largest resistor),
$v_o/(v_1 - v_2) = 11.26$]