Integrated differential amplifier

1-1 Difference Voltage

A differential amplifier is also called a difference amplifier, because it amplifies the difference between two signal voltages, (a difference voltage is the mathematical difference between two other voltages, each of whose values is given with respect to ground), for example, the collector-to-emitter voltage of a BJT is the difference between the collector-to-ground voltage and the emitter-to-ground voltage:

VCE = VC – VE----------1-1

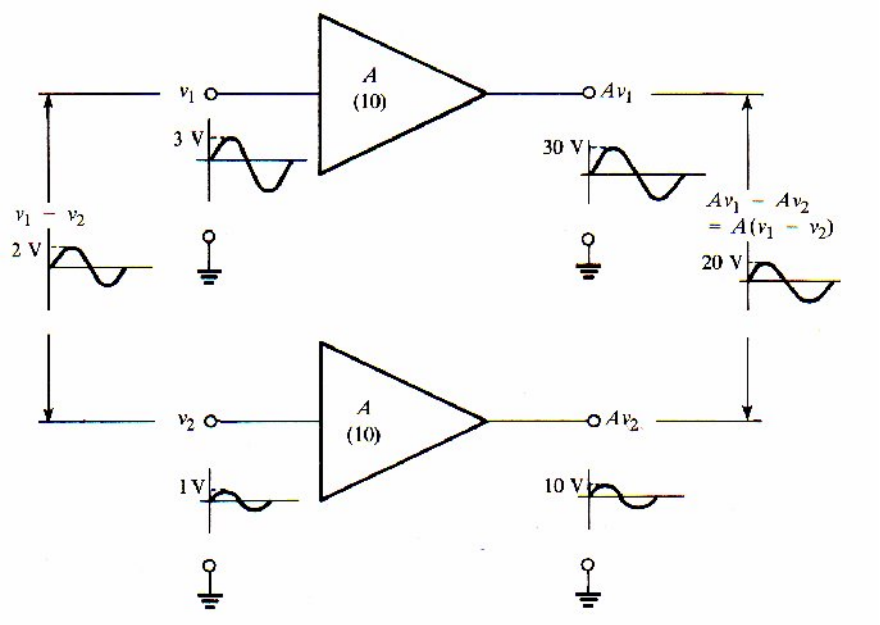


Fig1-1 The amplification of difference voltages

The two input voltages is v1 & v2, are shown as sine waves. the voltage gain of each amplifier is A, then vo1=Av1 & vo2= Av2 . The input difference voltage, v12 = v1 - v2, is a sine wave . the output difference voltage, Av1 - Av2 = A(v1 - v2).

1-2 The Ideal Differential Amplifier

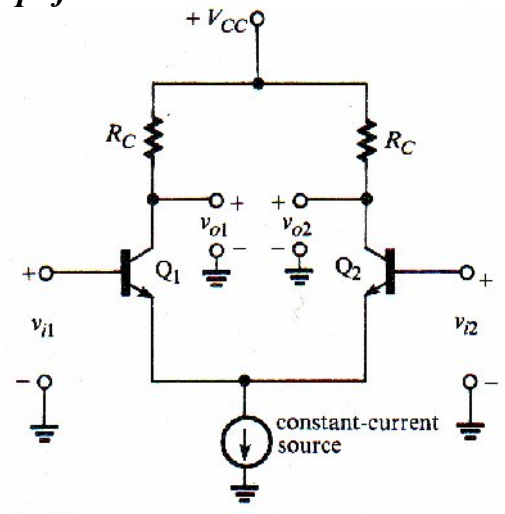


Fig1-2The basic BJT differential amplifier, the two transistors can be regard as CE amplifiers having a common connection at their emitter. The base terminals are the input to the differential and the collectors are the outputs

Figure 1-4 shows the amplifier with input 2 grounded (vi2 = 0) and a small signal applied to input 1. The ideal current source presents an infinite impedance (open circuit) to an ac signal. We also assume the ideal situation of perfectly matched transistors, so Q1 and Q2 have identical values of β, re . Since Q1 is CE amplifier, the voltage at its collector (vo1) is an amplified and inverted version of its input vi1. there is also an ac voltage ve1 developed at the emitter of Q1 this voltage is in phase with vi1

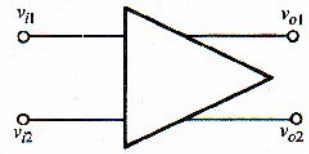


Fig1-3 Schematic symbol for the differential amplifier

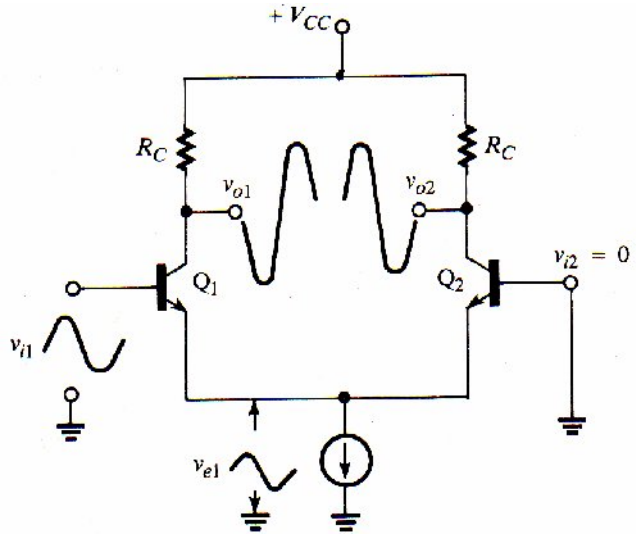


Fig1-4 The small signal voltages in a differential amplifier when one input is grounded, Note that ve1 is in phase with vi1 and vo1 is out of phase with vi1

The voltage ve1 is developed across the emitter resistance re looking into the emitter of Q2 (in parallel with the infinite resistance of the current source). Therefore, as far as the emitter-follower action of Q1 is concerned, the load resistance seen by Q1 is re . Since the emitter resistance of Q1 is itself re, then the emitter-follower gain is:

$$A_v = \frac{r_L}{r_L + r_e} = \frac{r_e}{r_e + r_e} = 0.5$$

ve1 is in phase with, and 1/2 the magnitude of vi1.
vbe2 = vb2 – ve1 = 0 – ve1, We see that even though the base of Q2 is grounded, there exists an ac base-to-emitter voltage on Q2 that is out of phase with ve1 and therefore out of phase with vi1.Consequently, there is an ac output voltage vo2 produced at the collector of Q2 and it is out of phase with vo1,Since both transistors are identical, they have equal gain and the output vo2 has the same magnitude as vo1. Since the emitter-follower gain of Q1 is 0.5,

ve is a 0.5(100 mV) = 50-mV-peak sine wave.

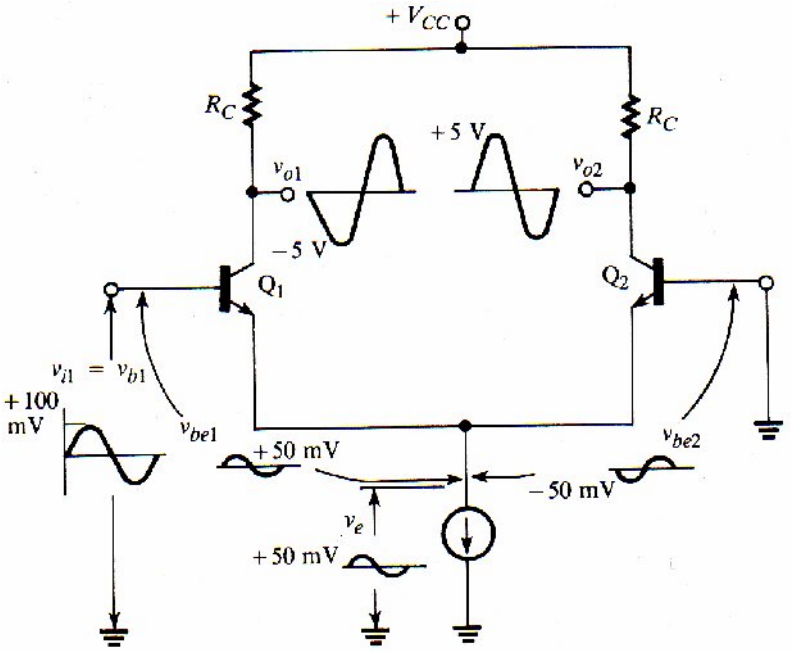


Fig1-5 Each transistor has identical voltage gain(-100) and the outputs at the collectors are -100 times their respective base-to-emitter voltage

vbe1= vb1 – ve1 = (100 mV) - (50 mV) = 50 mV.
vo1 = A x vbe1= -100(50 mV) = -5 V, an inverted 5-V-peak sine wave.
vbe2= vb2 - ve1 = 0 - (50 mV) = -50 mV .
vo2 =A x vbe2 = (-100)(- 50 mV) = + 5 V peak sine wave in phase with vi1 and out of phase with vo1.
the input difference voltage is vi1 – vi2 = (100 mV) - 0 = 100 mV peak.
the output difference voltage is 10V peak, since vo1 and vo2 are out of phase.
the magnitude of the difference voltage gain (vo1 - vo2)/(vi1 - vi2) =10 V/ 100 mV= 100.
the voltage gain vo/vi for each side is only 50, the difference voltage gain is the same as the gain vc/vbe of each transistor
the two inputs of a differential amplifier are driven by signals that are equal in magnitude and out of phase: vi2 = -vi1.
let us now ground input 1 (vi1 = 0) and assume that there is a signal applied to input 2 equal to and out of phase with the vi1 signal we previously assumed. vo2 is out of phase with vi1 and vo1 is in phase with vi2.
In figure 1-7, driving the two inputs with equal but out-of-phase signals . By superposition, each output is the sum of the voltages resulting from each input acting alone, so the outputs are exactly twice the level they would be if only one input signal were present.
In many applications, the output of a differential amplifier is taken from just one of the transistor collectors, vo1, for example. In this case the input is a difference voltage and the output is a voltage with respect to ground. This called single-ended output and the voltage gain in that mode is

$$A_{v(single\text{-}ended\ output)} = \frac{v_{o1}}{v_{i1} - v_{i2}} \qquad \text{------1-2}$$

the single-ended output gain is one-half the difference voltage gain (vo1 - vo2)/ (vi1 – vi2) which called as the double-ended voltage gain.

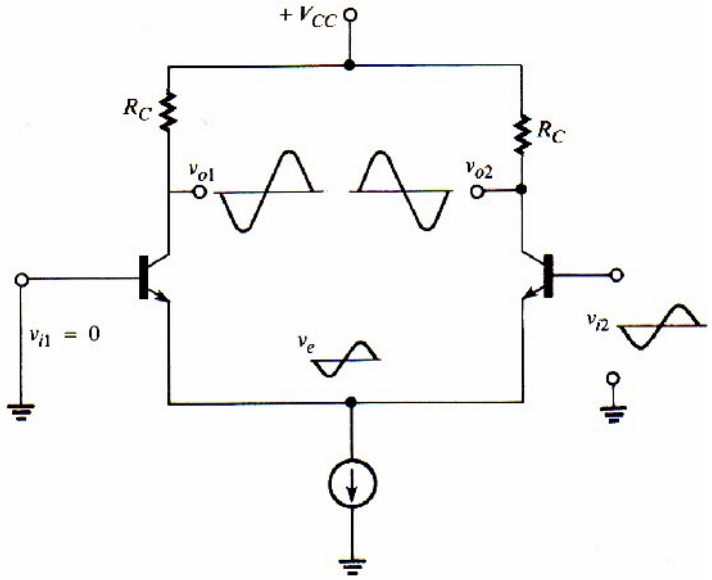


Fig1-6 The differential with vi1 grounded and a signal input vi2, campier with fig1-4 , Note that vi2 here is the opposite phase from vi1 in fig1-4 and that vo1 and vo2 are the same as in fig1-4

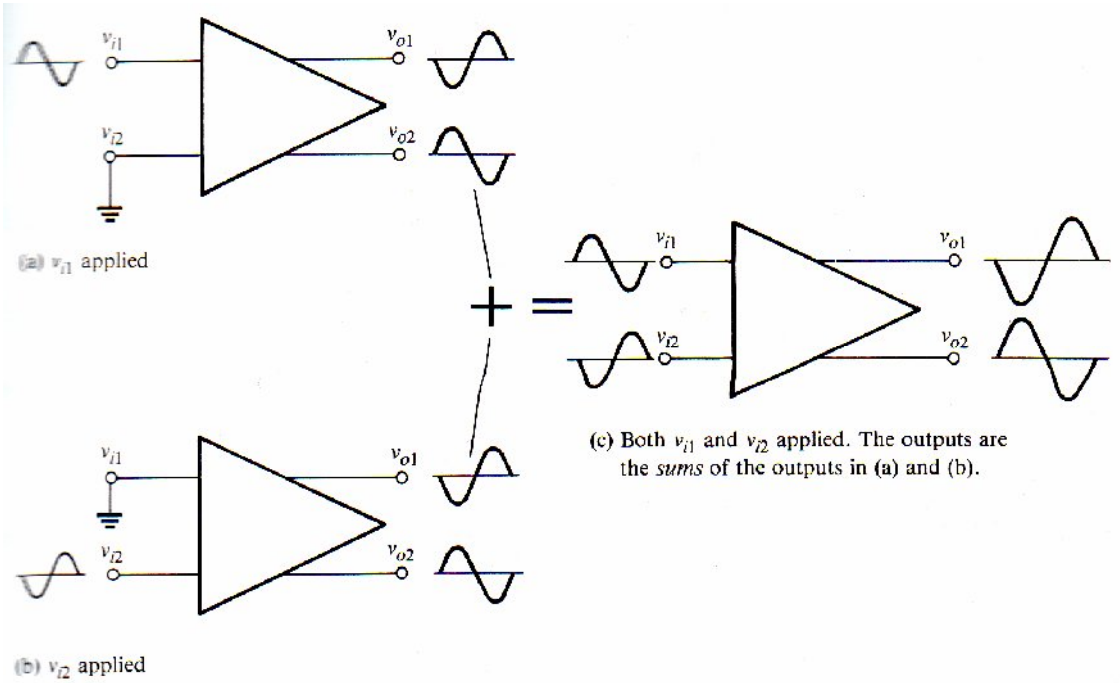


Fig1-7By the superposition principle, the output vo1 when both input are applied is the sum of the vo1 outputs due to each signal acting alone, likewise for vo2

Example 1-1. *The magnitude of the voltage gain (vc/vbe) for each transistor in Figure 1-2 is 100. If vi1 and vi2 are out-of-phase, 100-mV-peak signals applied simultaneously to the inputs, find*

I. the peak values of vo1 and v02,

2. the magnitude of the double-ended voltage gain (vo1 - vo2)/(vi1 – vi2), and
3. the magnitude of the single-ended output gain vo1/(vi1 – vi2).

Solution.

1. the peak value of each output = A x vbe1= 100 x 50 mV = 5V when one input is driven and the other is grounded.
Since the outputs are doubled when the inputs are equal and out of phase,

each output = 2 x 5 V = 10V peak.

2. Since vi1 = -vi2, the input difference voltage is vi1 - vi2 = 2vi1 = 200 mV peak.
vo1 = -vo2, so the output difference voltage is vo1 - vo2 = 2vo1 = 20 V peak . Therefore, the magnitude of (vo1 - vo2)/(vi1-vi2) = (20 V)/(200 mV)= 100.
3. The magnitude of the single-ended output gain is

$$|A_{v(\text{single-ended output})}| = \left|\frac{v_{o1}}{v_{i1} - v_{i2}}\right| = \frac{10\text{ V}}{200\text{ mV}} = 50$$

vo1 is out of phase with (vi1 - vi2), the correct specification for the single-ended output gain is -50. If the single-ended output is taken from the other side (vo2), which is out of phase with vo1, then the gain vo2/(vi1- vi2) = +50.

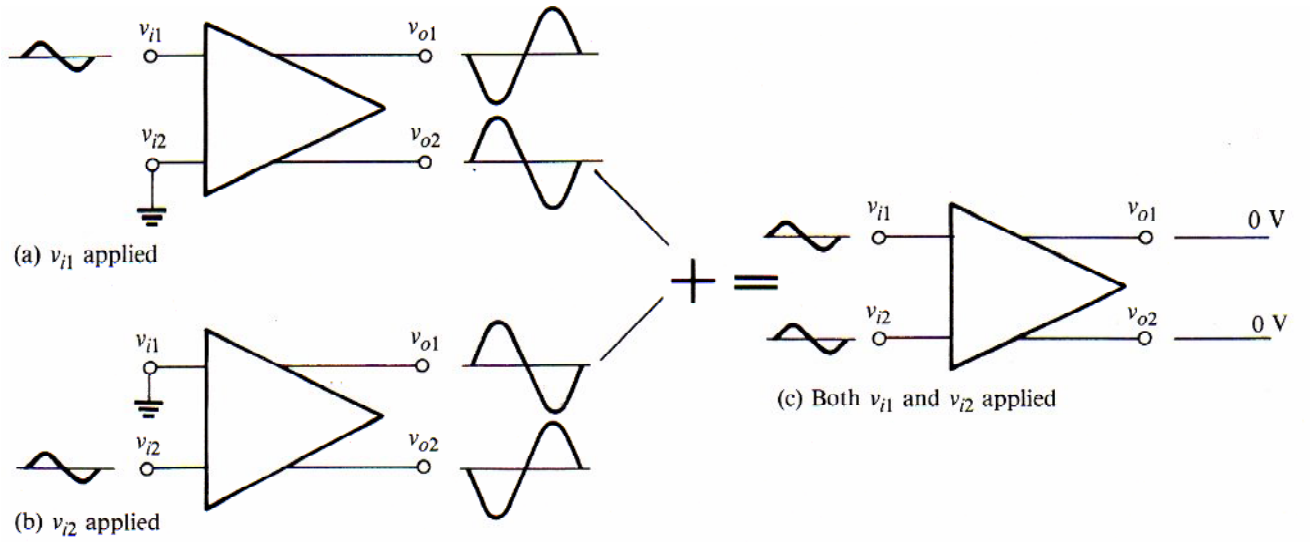


Fig1-8 the output of the differential amplifier are 0 when the two inputs are equal and in phase

Since the output difference voltage vo1 - vo2 is out of phase with the input difference voltage vi1 - vi2, the correct specification for the double-ended voltage gain is -100.
if the two inputs are driven by equal in-phase signals, the output at each collector will be exactly 0, and the output difference voltage will be 0, the input difference voltage is also 0.
We are again assuming that the current source has infinite resistance. Neglecting the output resistance ro at the collector of Q1, we can use the familiar approximation for the voltage gain of the transistor:

$$\frac{v_{o1}}{v_{be1}} \approx \frac{-R_C}{r_e} \qquad \text{----------1-3}$$

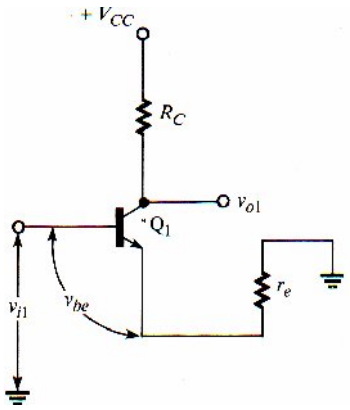


*Fig1-9 when the input to Q2 is grounded, there is resistance **re** in series with the emitter of Q1*

where re is the emitter resistance of Q1. It is clear from Figure 1-9 that the voltage gain vo1/vi1 is

$$\frac{v_{o1}}{v_{i1}} \approx \frac{-R_C}{2r_e} \quad \text{----------1-4}$$

2re is in the denominator because we assume re1=re2, i.e. double-ended voltage gain

$$\frac{v_{o1} - v_{o2}}{v_{i1} - v_{i2}} \approx \frac{-R_C}{r_e} \quad \text{----------1-5}$$

single-ended output voltage gain

$$\frac{v_{o1}}{v_{i1} - v_{i2}} \approx \frac{-R_C}{2r_e} \quad \text{----------1-6}$$

that vo1 and vo2 will always have the same amplitude and be out of phase with each other. Thus,

$$\frac{v_{o2}}{v_{i1} - v_{i2}} \approx \frac{R_C}{2r_e} \quad \text{----------1-7}$$

The small-signal differential input resistance is defined to be the input difference voltage divided by the total input current. Since the total small-signal resistance in the path from one input through both emitters to the other input is 2re, the differential input resistance is

$$r_{id} = 2(\beta + 1)\, r_e \quad \text{----------1-8}$$

*Since the transistors are identical, the source current **I** divides equally between them, and the emitter current in each is therefore*

$$I_E = I_{E1} = I_{E2} = I/2 \quad \text{----------1-9}$$

The dc output voltage at the collector of each transistor is

$$V_{o1} = V_{CC} - I_{C1}R_C$$

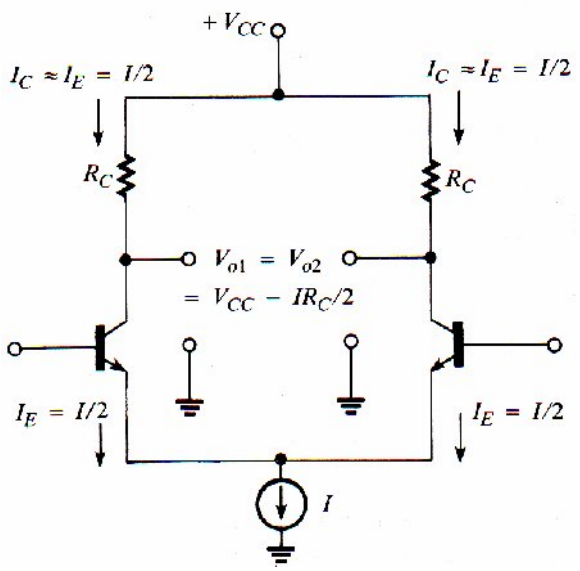
$$V_{o2} = V_{CC} - I_{C2}R_C$$

Since $I_C \approx I_E = I/2$ in each transistor, we have

$$V_{o1} = V_{o2} \approx V_{CC} - (I/2)R_C \quad \text{----------1-10}$$

the familiar approximation re ≈ 0.026/IE we obtain

$$r_{e1} = r_{e2} = r_e \approx \frac{0.026}{I_E} = \frac{0.026}{I/2} \quad \text{---------1-11}$$



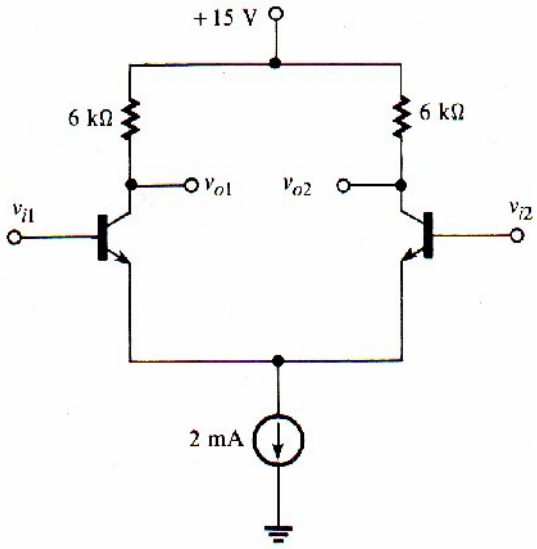


Fig1-10 DC voltage and currents in an ideal differential Amp *Fig1-11 Example1-2*

Example 1-2. *For the ideal differential amplifier shown in Figure 1-11, find*
1. the dc output voltages vo1 and vo2,
2. the single-ended output gain vo1/(vi1 – vi2), and
3. the double-ended gain (vo1 - vo2)/(vi1 – vi2).

Solution.

1. The emitter current in each transistor is IE = I/2 = (2 mA)/2 = 1 mA ≈ Ic. Therefore,
vo1 = vo2 = Vcc - IcRc = 15 - (1 mA)(6 kΩ) = 9 V.

2. The emitter resistance of each transistor is

$$r_e \approx \frac{0.026}{I_E} = \frac{0.026}{1\text{ mA}} = 26\ \Omega$$

Therefore, from equation 1-6

$$\frac{v_{o1}}{v_{i1} - v_{i2}} \approx \frac{-R_C}{2r_e} = \frac{-6\text{ k}\Omega}{52\ \Omega} = -115.4$$

3.from equation1-5

$$\frac{v_{o1} - v_{o2}}{v_{i1} - v_{i2}} = \frac{-R_C}{r_e} = \frac{-6\text{ k}\Omega}{26\ \Omega} = -230.8$$

1-2 Common-Mode Parameters

One attractive feature of a differential amplifier is its ability to reject signals that are common to both inputs. Since the outputs are amplified versions of the difference between the inputs, any voltage component that appears identically in both signal inputs will be "differenced out" that is, will have zero level in the outputs. Any dc or ac voltage that appears simultaneously in both signal inputs is called a common-mode signal vcm. The ability of an amplifier to suppress, or zero-out, common-mode signals is called common-mode rejection. The differential common-mode gain Acm, is defined to be the ratio of the output difference voltage caused by the common-mode signal to the common-mode signal itself:

$$A_{cm} = \frac{(v_{o1} - v_{o2})_{cm}}{v_{cm}} \qquad \text{----------1-12}$$

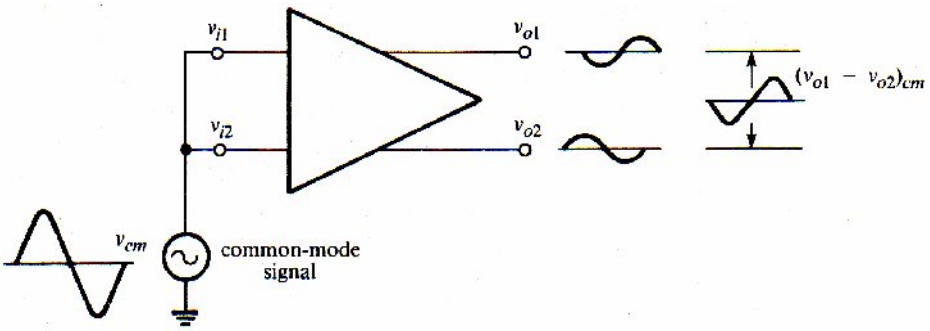


Fig1-12 if the differential amplifier were ideal, both outputs would be 0 when the inputs have the same(common-mode) signal, in reality, there is a small common-mode output, as shown

Obviously the ideal amplifier has common-mode gain equal to 0.
Common-mode rejection ratio (CMRR), defined to be the ratio of the magnitude of its - differential (difference-mode) gain Ad to the magnitude of its common-mode gain

$$\text{CMRR} = \frac{|A_d|}{|A_{cm}|} \text{----------1-13}$$

The value of the CMRR is often given in decibels:

$$\text{CMRR} = 20 \log_{10} \left| \frac{A_d}{A_{cm}} \right| \text{----------1-14}$$

***Example 1-3**. When the inputs to a certain differential amplifier are vi1 = 0.1sin wt and vi2 = -0.1 sin wt, it is found that the outputs are vo1 = -5 sin wt and vo2 = 5 sin wt. When both inputs are 2 sin wt, the outputs are vo1 = -0.05 sin wt and vo2 = 0.05 sin wt. find the CMRR in dB.*
***Solution.** We will use the peak values of the various signals for our gain computations, but note carefully how the minus signs are used to preserve phase relations , the difference-mode gain is*

$$A_d = \frac{v_{o1} - v_{o2}}{v_{i1} - v_{i2}} = \frac{-5 - 5}{0.1 - (-0.1)} = \frac{-10}{0.2} = -50$$

The common-mode gain is

$$A_{cm} = \frac{(v_{o1} - v_{o2})_{cm}}{v_{cm}} = \frac{-0.05 - 0.05}{2} = \frac{-0.1}{2} = -0.05$$

The common-mode rejection ratio is

$$\text{CMRR} = \frac{|A_d|}{|A_{cm}|} = \frac{50}{0.05} = 1000$$

Expressing this result in dB, we have CMRR

$$\text{we have CMRR} = 20 \log_{10}(1000) = 60 \text{ dB}.$$

1-3 Practical Differential Amplifier
Our gain derivations for the ideal differential amplifier were based on the assumption that both transistors had identical values of re Clearly, the voltage gains of both sides will not be identical if the values of re are not, in which case the outputs will not truly represent amplified versions of the input difference voltage, and the CMRR will suffer. To reduce the

effect of variations in re, equal-valued resistors RE can be inserted in series with the emitters, as shown in Figure 1-13.

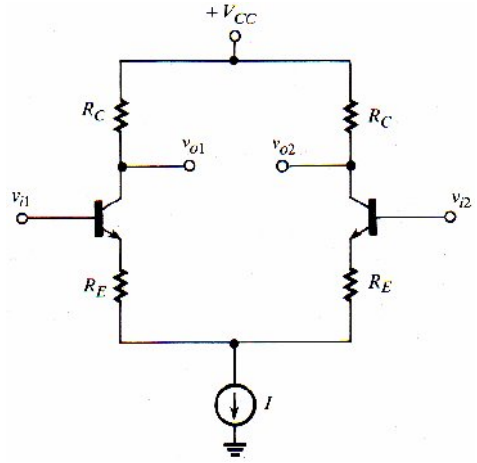


Fig1-13 Inserting a resistance RE in series with each emitter reduces the amplifiers dependence on matched re values

Equations 1-5 and 1-6, modified for the inclusion of RE, become

$$\frac{v_{o1} - v_{o2}}{v_{i1} - v_{i2}} \approx \frac{-R_C}{r_e + R_E} \approx \frac{-R_C}{R_E} \quad \text{if } R_E >> r_e$$

----------1-15

$$\frac{v_{o1}}{v_{i1} - v_{i2}} \approx \frac{-R_C}{2(r_e + R_E)} \approx \frac{-R_C}{2R_E} \quad \text{if } R_E >> r_e$$

----------1-16

Equation 1-8 becomes

$$r_{id} = 2(\beta + 1)(r_e + R_E)$$

----------1-17

Figure 1-14 shown Another reality in practical differential amplifiers is that the current source biasing the amplifier does not have infinite resistance, the current-source resistance in each half-circuit must be 2R and the value of the current must be I/2 to maintain equivalence.

The voltage gain of Q1 is

$$\frac{v_{o1}}{v_{cm}} \approx \frac{-R_C}{r_e + 2R}$$

----------1-18

And that of Q2 is

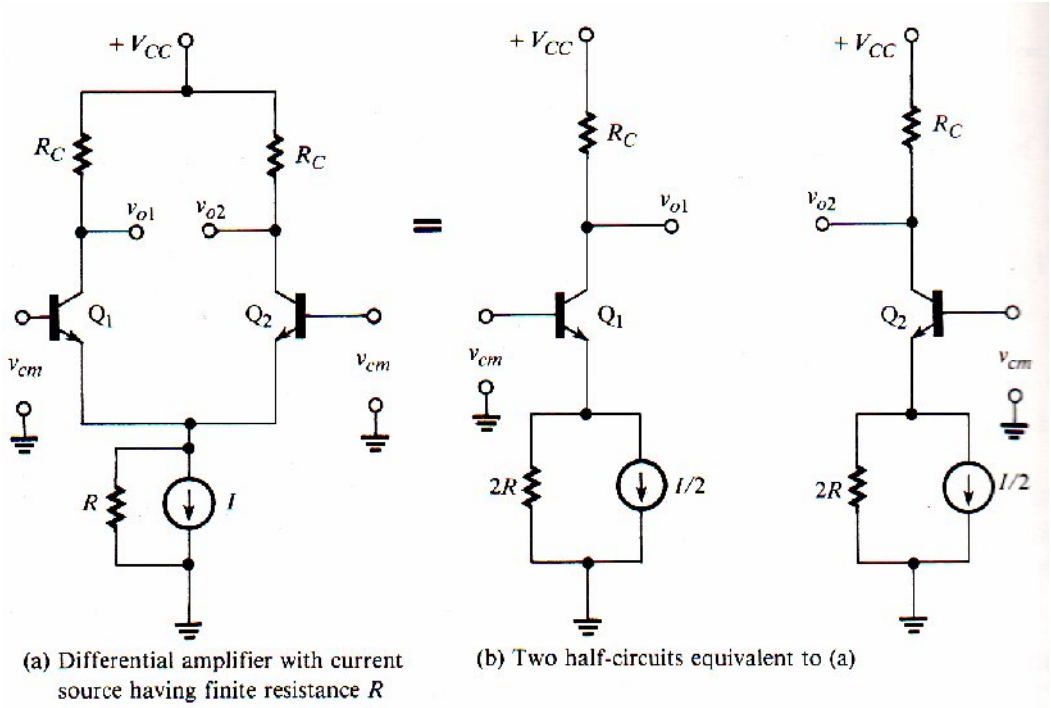
$$\frac{v_{o2}}{v_{cm}} \approx \frac{-R_C}{r_e + 2R}$$

----------1-19

Therefore

$$A_{cm} = \frac{(v_{o1} - v_{o2})_{cm}}{v_{cm}} = \frac{-R_C}{r_e + 2R} - \frac{-R_C}{r_e + 2R} = 0$$

This shows that the differential common-mode gain is unaffected by source resistance R .



(a) Differential amplifier with current source having finite resistance R

(b) Two half-circuits equivalent to (a)

Fig1-14 Analyzing the effect of source resistance R on common-mode behavior

1-4 Bias Methods in Integrated Circuits

integrated-circuit amplifiers use transistor constant-current sources, an example of which is illustrated in Figure 1-15. Transistor Q3 has a large output resistance at its collector therefore assuming that (βR_{E3})>>(R1 ‖ R2), the base voltage of Q3 is

$$V_{B3} = -V_{EE}\left(\frac{R_2}{R_1 + R_2}\right) \text{----------1-20}$$

Assuming a silicon transistor, the emitter voltage of Q3 is

$$V_{E3} = V_{B3} - 0.7 \text{ ----------1-21}$$

$$I_{E3} = \frac{|V_{EE}| - |V_{E3}|}{R_{E3}} \text{ ----------1-22}$$

Example1-4 *Transistor Q3 in fig1-16 has β=100.Assuming that Q1 and Q2 are matched, find approximate values for*

1-the emitter current in Q1 and Q2, and

2-the dc output voltage vo1 and vo2

Solution. *1-*

$$V_{B3} = \left[\frac{10\text{ k}\Omega}{(10\text{ k}\Omega) + (4.7\text{ k}\Omega)}\right](-15\text{ V}) = -10.2\text{ V}$$

$$V_{E3} = -10.2 - 0.7 = -10.9\text{ V}$$

$$I_{E3} = \frac{(15 - 10.9)\text{ V}}{4\text{ k}\Omega} = 1\text{ mA} \approx I_{C3}$$

$$I_{E1} = I_{E2} = I_{C3}/2 = 0.5\text{ mA}$$

2-

$$I_{C1} = I_{C2} \approx I_{E1} = I_{E2} = 0.5\text{ mA}$$

$$V_{o1} = V_{o2} = 15 - (0.5\text{ mA})(10\text{ k}\Omega) = 10\text{ V}$$

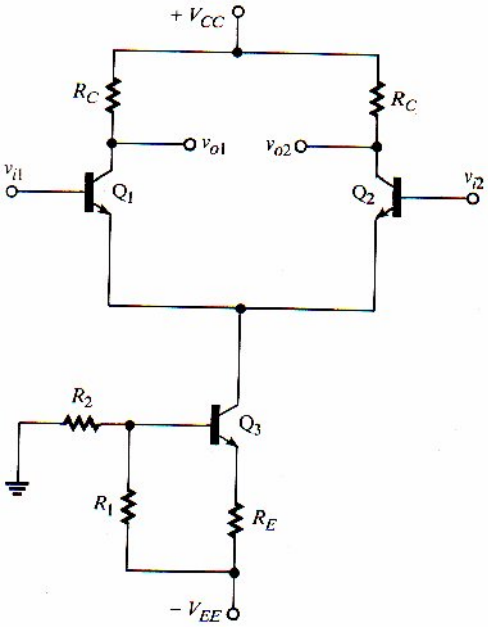


Fig1-15 a transistor current source used to bias a differential Amp

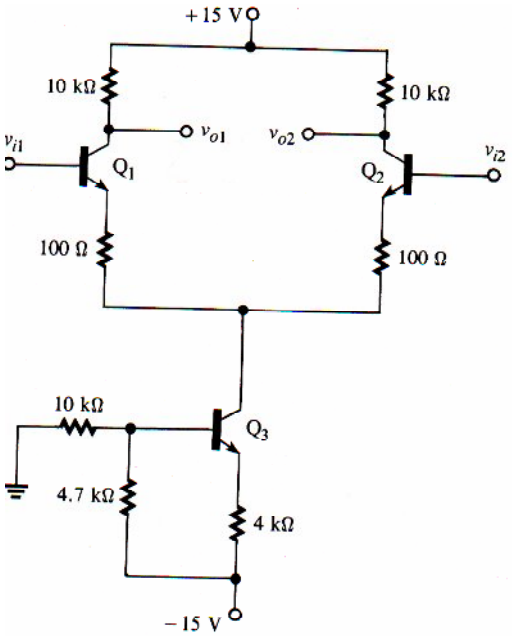


fig1-16 example(1- 5)

Example1-5 *Assuming that each of Q1 and Q2 in Figure 1-16 has β =100 and that the output resistance at the collector of Q3 is 500 kΩ, find*

1. the differential input resistance,

2. the single-ended common-mode gain, and

3. the single-ended common-mode rejection ratio.

Solution: *The small-signal emitter resistance of Q1 and Q2 is*

1- the small-signal emitter resistance of Q1 and Q2 is

$$r_e \approx \frac{0.026}{I_E} = \frac{0.026}{0.5\text{ mA}} = 52\ \Omega$$

$$, r_{id} = 2(\beta + 1)(r_e + R_E) = 2(101)(52 + 100) = 30.7\ \text{k}\Omega.$$

Equations 1-18 &1-19 are for the case RE =0. When resistance RE is included each emitter circuit, the single-ended common-mode gain is

$$\frac{-R_C}{r_e + R_E + 2R} = \frac{-10^4}{52 + 100 + (2)(0.5 \times 10^6)} \approx -10^{-2}$$

3. from equation 1-16 the single-ended output gain is

$$\frac{-R_C}{2(r_e + R_E)} = \frac{-10^4}{2(52 + 100)} = -32.9$$

Therefore, the single-ended CMRR is

$$\frac{32.9}{10^{-2}} = 3290 \qquad \textit{Or 70.3 dB}$$

1-6 Introduction to Operational Amplifiers

An operational amplifier is basically a differential amplifier modified by the addition of circuitry that improves its performance and gives it certain special features. The most important characteristics of an operational amplifier are listed below:

1. It is a dc (direct-coupled, direct-current) amplifier.
2. It should have a very large voltage gain-ideally, infinite.
3. It should have a very large input impedance-ideally, infinite.
4. It should have a very small output impedance-ideally zero.
5. The output should be exactly zero V when the inputs are zero V.
6. The output must be capable of both positive and negative voltage swings.
7. It should have a very large CMRR.
8. It is operated with a single-ended output and differential input (although one input is often grounded,).
9. It should meet whatever special requirements are demanded by a particular application these include parameters such as noise level, frequency response, and slew rate.
The name operational amplifier is derived from amplifier applications that the performance of precise mathematical operations on input signals, including voltage summation, subtraction, and integration.
The input stage of every operational amplifier is a differential amplifier. To achieve a large input impedance, Components in the input stage should be very closely matched to achieve the best possible balance in the differential operation. This is important to ensure that the output of the operational amplifier is a precise representation of the input difference voltage, that the output is exactly zero when the inputs are zero, and that the CMRR is large. voltage gain is achieved through the use of multistage amplifier. To permit the output voltage to swing through both positive and negative values, both a positive and a negative supply voltage are required. These are usually equal-valued, opposite-polarity supplies, a typical example being ± 15 V.

Circuit Analysis of an Operational Amplifier
Example1-6 *Figure 1-17 shows a simple operational amplifier that we can use as an example to analyzed important function components discussed*

$$V_{B7} = \left[\frac{10\ \text{k}\Omega}{(10\ \text{k}\Omega) + (4.7\ \text{k}\Omega)}\right](-15\ \text{V}) = -10.2\ \text{V}$$

VE7= V B7 - 0.7 = - 10.9 V,

$$I_{E7} = \frac{|V_{EE}| - |V_{E7}|}{R_{E7}} = \frac{(15 - 10.9)\text{V}}{10.2\ \text{k}\Omega} = 0.4\ \text{mA}$$

IC1 = IC2 = IE1= IE2 = (0.4 mA)/2 = 0.2 mA,
VC1=VC2= Vcc -IcRc = 15 - (0.2 mA)(25 kΩ) = 10 V.
VE1=VE2= 0 - 0.7 = -0.7 V,

the small drop across each 50-Ω resistor [(50) x (0.2 mA) = 0.01 V] sets the collector of Q7 at about the same voltage (-0.71 V).
Since VB8 = VB7 = -10.2 V, i.e. VE8= VB8 - 0.7 = -10.9 V. Then

$$I_{E8} = \frac{|V_{EE}| - |V_{E8}|}{R_{E8}} = \frac{(15 - 10.9)\text{V}}{2.27\ \text{k}\Omega} = 1.8\ \text{mA}$$

The 1.8 mA divides equally between Q3 and Q4, so VC4 = Vcc - IcRc = 15 - (0.9 mA)(3.3 kΩ) = 12 V.
Since the bases of Q3 and Q4 are direct-coupled to the collectors of Q1 and Q2,

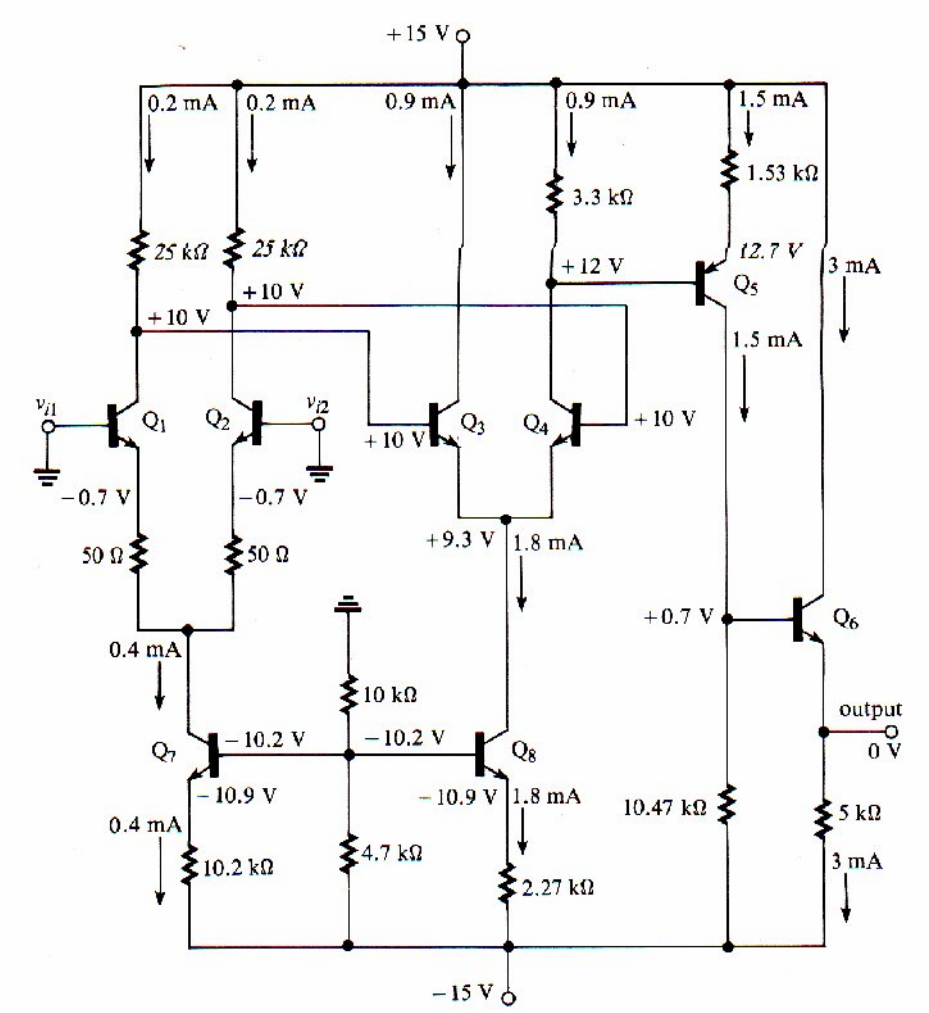


Figure 1-17 A simple operational amplifier incorporating deferential, gain. And level-shifting stages. All voltages shown are dc levels with respect to ground

$$VB3 = VB4 = 10\ V.$$
$$VE3 = VE4 = 10 - 0.7 = 9.3\ V.$$
$$VB5 = 12\ V.\ \text{Therefore,}\ \ VE5 = VB5 + 0.7 = 12.7\ V.$$
$$I_{E5} = \frac{V_{CC} - V_{E5}}{R_{E5}} = \frac{(15 - 12.7)\text{V}}{1.53\ \text{k}\Omega} = 1.5\ \text{mA}$$

Since IC5 = IE5, VC5 = (IC5)(10.47 kΩ) - VEE = (1.5 mA)(10.47 kΩ) - 15 = +0.7 V. Since the base of the output transistor, Q6, is at 0.7 V, its emitter is at 0 V, and the amplifier output is 0 V. The bias current in Q6 is (0 - VEE)/5 kΩ = (15 V)/ (5 kΩ) = 3 mA.

Example 1-7. *Assume that the transistors in Figure 1-17 are matched and that all have β=100. Neglecting the collector output resistance of each transistor, find*
1. the voltage gain Vo/(Vi1 – Vi2),
2. the differential input resistance of the amplifier,
3. the output resistance of the amplifier.
Solution.

1. The load driven by the input differential stage is the differential input resistance rid34 of the second stage. Since IE3 = IE4 = 0.9 mA,

$$r_{e3} = r_{e4} \approx \frac{0.026}{0.9\text{ mA}} = 28.9\ \Omega$$

Therefore, rid34 = β (re3 + re4) = 100(28.9 + 28.9) = 5.78 kΩ.

The ac equivalent circuit of the first stage is shown in Figure 1-18. The double ended voltage gain is given by

$$\frac{v_{o1} - v_{o2}}{v_{i1} - v_{i2}} = \frac{-(\text{resistance in collector circuit})}{\text{resistance in emitter circuit}} \qquad \text{-------1-23}$$

$$= \frac{-(R_{C1} + R_{C2}) \parallel r_{id34}}{2R_E + r_{e1} + r_{e2}}$$

Since $I_{E1} = I_{E2} = 0.2$ mA,

$$r_{e1} = r_{e2} \approx \frac{0.026}{0.2\text{ mA}} = 130\ \Omega$$

Thus,

$$\frac{v_{o1}}{v_{i1} - v_{i2}} = \frac{-[(25\text{ k}\Omega) + (25\text{ k}\Omega)] \parallel (5.78\text{ k}\Omega)}{2(50\ \Omega) + (130\ \Omega) + (130\ \Omega)} = -14.4$$

The ac load resistance driven by the second stage is the input resistance looking into the base of Q5:

ri5 = β (re5 + RE5). Since IE5 = 1.5 mA, re5 = 0.026/(1.5 mA) = 17.3 Ω.

Thus, ri5 = 100[(17.3 Ω) + (1.53 kΩ)] = 154.73 kΩ.

The second stage is operated single-ended and its gain is

$$\frac{v_{o4}}{v_{i3} - v_{i4}} = \frac{R_{C4} \parallel r_{i5}}{r_{e3} + r_{e4}} = \frac{(3.3\text{ k}\Omega) \parallel (154.73\text{ k}\Omega)}{(28.9\ \Omega) + (28.9\ \Omega)} = 55.9$$

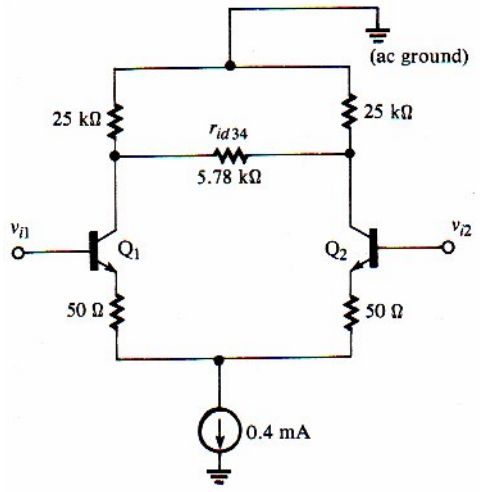


Figure 1-8 (Example 1-7) The ac equivalent circuit of the input stage, showing the differential input resistance of the second stage connected between the collectors

The resistance in the collector circuit of the level-shifting stage (Q5) is (10.47 kΩ) ‖ ri6, where ri6 is the input resistance looking into the base of Q6,

Since IE6 = 3 mA, re6 = 0.026/(3 mA) = 8.70

and ri6 = β (re6 + RE6) = 100[(8.70)+ (5 kΩ)] = 500 kΩ.

Thus, the gain of Q5 is

$$\frac{v_{o5}}{v_{o4}} = \frac{-(10.47\ \text{k}\Omega) \parallel r_{i6}}{R_{E5} + r_{e5}} = \frac{-(10.47\ \text{k}\Omega) \parallel (500\ \text{k}\Omega)}{(1.53\ \text{k}\Omega) + (17.3\ \Omega)} = -6.6$$

Finally, the gain of the emitter-follower output stage is

$$\frac{v_{o6}}{v_{o5}} = \frac{r_{L6}}{r_{L6} + r_{e6}} = \frac{5\ \text{k}\Omega}{(5\ \text{k}\Omega) + (8.7\ \Omega)} \approx 1$$

The overall gain of the amplifier is the product of the gain calculated for the stages

$$\frac{v_o}{v_{i1} - v_{i2}} = (-14.4)(55.9)(-6.6)(1) = 5312$$

(This would not be considered a very large voltage gain for modem operational amplifiers.)

2. The differential resistance looking into the first stage is

rid12 = β (re1 + re2 + 2RE) = 100(130 + 130 + 100) = 36 kΩ.

3. Recall that the output resistance of an emitter-follower stage is

$$r_o(\text{stage}) = R_E \left\| \left(r_e + \frac{R_B \parallel r_S}{\beta + 1} \right) \right.$$

$R_B \parallel r_S = (10.47\ \text{k}\Omega) \parallel r_o(\text{Q}_5) = 10.47\ \text{k}\Omega$. Therefore,

$$r_o = (5\ \text{k}\Omega) \left\| \left[(8.7\ \Omega) + \frac{10.47\ \text{k}\Omega}{101} \right] \right. = 112\ \Omega$$

2- The Ideal Operational Amplifier

an operational amplifier is a direct-coupled amplifier with two (differential) inputs and a single output having the following attributes

1. It has infinite gain.

2. It has infinite input impedance.

3. It has zero output impedance.

Figure 2-1 shows the standard symbol for an operational amplifier the two inputs are labeled " + " and " - " correspondingly to vi^+ & vi^- these correspond to vi1& vi2, the + input is the noninverting input and the - input is the inverting input. The idea of many applications of operational amplifiers are summarized in the table accompanying Figure 2-1.

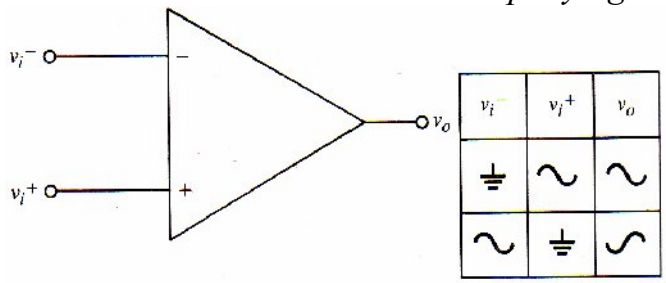


Figure 2-1 Operational amplifier symbol, showing inverting (-) and noninverting (+) inputs

2-1 The Inverting Amplifier

Figure 2-2 is a very useful application of an operational amplifier, the noninverting input is grounded, vin is connected through R1 to the inverting input, and feedback resistor Rf is connected between the output and vi^-. Since we are using the amplifier in an inverting mode, we denote the voltage gain by -A, vin ≠ vi^-, we define

$$v_o = -Av_i^- \quad \text{----------2-1}$$

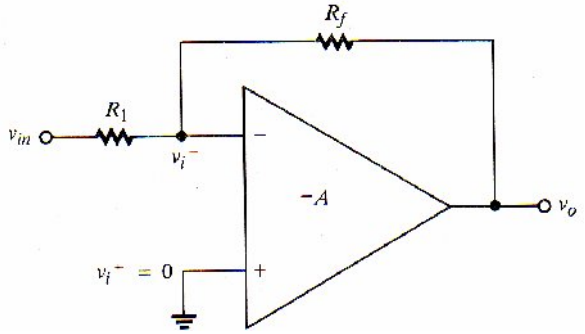


Fig 2-2 An operational-Amplifier application in which signal vin is connected through R1. Resistor Rf provides feedback, vo/vi^- = -A

from Ohm's law, the current i1 is simply the difference in voltage across R1, divided by R1

$$i_1 = (v_{in} - v_i^-)/R_1 \quad \text{----------2-2}$$

Similarly, the current if is the difference in voltage across Rf divided by Rf

$$i_f = (v_i^- - v_o)/R_f \quad \text{----------2-3}$$

Writing Kirchhoff's current law at the inverting input, we have

$$i_1 = i_f + i^- \quad \text{----------2-4}$$

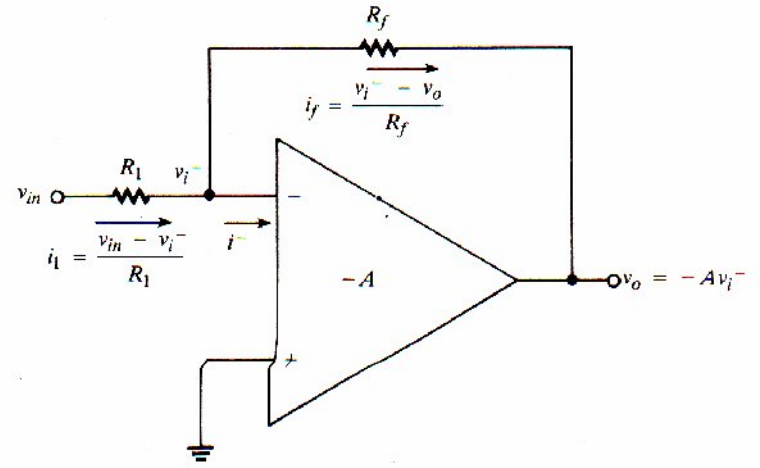


Figure 2-3 Voltages and currents resulting from the application of the signal voltage vin

i^- is the current entering the amplifier at its inverting input, the ideal amplifier has infinite input impedance, which means i^- must be 0. So (2-4) is simply

$$i_1 = i_f \quad \text{----------2-5}$$

Substituting (2-2) and (2-3) into (2-5) gives

$$\frac{v_{in} - v_i^-}{R_1} = \frac{v_i^- - v_o}{R_f}$$

or

$$\frac{v_{in}}{R_1} - \frac{v_i^-}{R_1} = \frac{v_i^-}{R_f} - \frac{v_o}{R_f} \quad \text{----------2-6}$$

From the definition(equation 2-1)

$$v_i^- = -\frac{v_o}{A} \quad \text{----------2-7}$$

If we Now invoke the assumption that $|A| = \infty$, we see that –vo/A=0, and therefore

$$v_i^- = 0 \quad \text{(ideal amp, with } |A| = \infty) \quad \text{----------2-8}$$

Substituting $vi^- = 0$ into (2-6) gives

$$\frac{v_{in}}{R_1} = \frac{-v_o}{R_f}$$

or

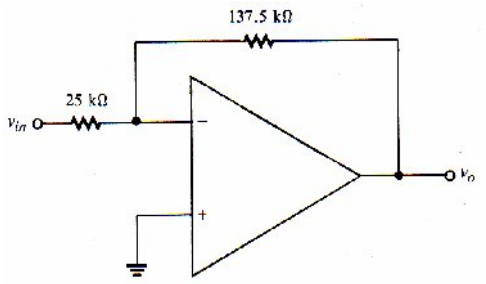
$$\frac{v_o}{v_{in}} = \frac{-R_f}{R_1} \quad \text{----------2-9}$$

(2-9)the gain is negative, meaning that the configuration is an inverting amplifier, also the magnitude of vo/vin depends only on the ratio of the resistor values . The gain vo/vin is a closed-loop gain of the amplifier, while A is called the open-loop gain.

***Example 2-1**. Assuming that the operational amplifier in Figure2-4 is ideal, find*
1. the rms value of vo when vin is 1.5 V rms,

2. the rms value of the current in the 25-kΩ resistor when vin is 1.5 V rms, and
3. the output voltage when vin = -0.6 V dc.

Solution:



$$\frac{v_o}{v_{in}} = \frac{-R_f}{R_1} = \frac{-137.5\ \text{k}\Omega}{25\ \text{k}\Omega} = -5.5$$

Figure 2-4 Example2-1

Thus, $|v_o| = 5.5|v_{in}| = 5.5(1.5\ \text{V rms}) = 8.25\ \text{V rms}$

2. Since $v_i^- \approx 0$(virtual ground) the current in the 25kΩ resistor is

$$i = \frac{v_{in}}{R_1} = \frac{1.5\ \text{V rms}}{25\ \text{k}\Omega} = 60\ \mu\text{A rms}$$

3. $v_o = (-5.5)v_{in} = (-5.5)(-0.6) = 3.3\ \text{V dc}.$

The output is a positive dc voltage when the input is a negative, and vice versa

2-3 The Noninverting Amplifier

Figure 2-5 shows another useful application of an operational amplifier, called the noninverting configuration.

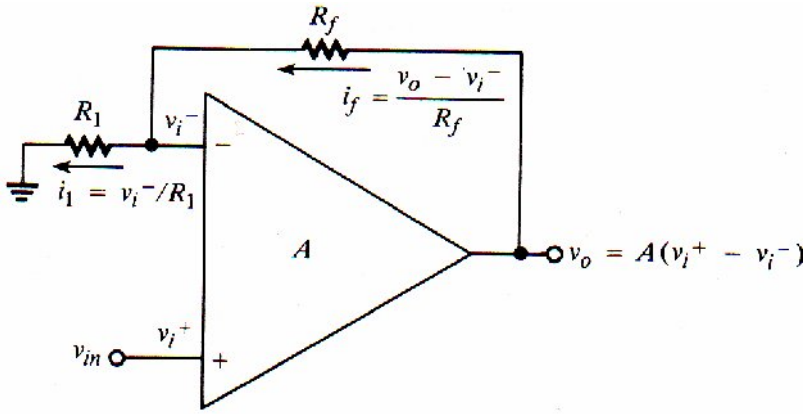


Figure2-5 The operational amplifier in a noninverting configuration

The input signal vin is connected directly to the noninverting input and R1 is connected from the inverting input to ground. Under the ideal assumption of infinite input impedance, no current flows into the inverting input, so i1 = if . Thus,

$$\frac{v_i^-}{R_1} = \frac{v_o - v_i^-}{R_f} \quad \text{----------2-10}$$

$$v_o = A(v_i^+ - v_i^-) \quad \text{----------2-11}$$

Solving 2-11 for v_i^- gives

$$v_i^- = v_i^+ - v_o/A \quad \text{----------2-12}$$

Letting A= ∞, the term vo/A = 0 and we have

$$v_i^- = v_i^+ \quad \text{----------2-13}$$

Substituting vi^+ for vi^- in (2-10) gives

$$\frac{v_i^+}{R_1} = \frac{v_o - v_i^+}{R_f} \quad \text{----------2-14}$$

Solving for vo/vi^+ and recognizing that $vi^+ = vin$ lead to

$$\frac{v_o}{v_{in}} = 1 + \frac{R_f}{R_1} = \frac{R_1 + R_f}{R_1} \quad \text{----------2-15}$$

From (2-8) when an operational amplifier is connected in an inverting configuration, with $vi^+=0$, the assumption $|A| = \infty$ gives $vi^- =0$ (ground), i.e., $vi^- = vi^+$. Also, in the non inverting configuration, the same assumption gives the same result: $vi^- = vi^+$ (2-13).

(2-15) shows that the closed-loop gain of the noninverting amplifier, like that of the inverting amplifier, depends only on the values of external resistors.A further advantage of the noninverting amplifier is that the input impedance seen by vin is infinite, so the closed-loop gain is vo/vin=1+Rf/R1=1. This configuration is called a voltage follower because vo has the same magnitude and phase as vin.

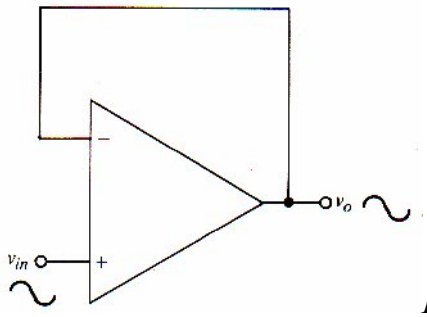


Figure 2-6 The voltage follower

***Example 2-2**. In a certain application, a signal source having 60 kΩ of source impedance produces a 1-V-rms signal. This signal must be amplified to 2.5-V-rms and drive a 11-kΩ load. Assuming that the phase of the load voltage is of no concern, design an operational-amplifier circuit for the application*

***Solution**. Since phase is of no concern and the required voltage gain is greater than 1, we can use either an inverting or noninverting amplifier. Suppose we decide to use the inverting configuration and arbitrarily choose Rf = 250 kΩ. Then,*

$$\frac{R_f}{R_1} = 2.5 \Rightarrow R_1 = \frac{R_f}{2.5} = \frac{250\ \text{k}\Omega}{2.5} = 100\ \text{k}\Omega$$

$$v_{in} = \left(\frac{R_1}{R_1 + r_S}\right)(1\ \text{V rms}) = \left[\frac{100\ \text{k}\Omega}{(100\ \text{k}\Omega) + (60\ \text{k}\Omega)}\right](1\ \text{V rms}) = 0.625\ \text{V rms}$$

$$v_o = \frac{R_f}{R_1}(0.625\ \text{V rms}) = \frac{250\ \text{k}\Omega}{100\ \text{k}\Omega}(0.625\ \text{V rms}) = 1.5625\ \text{V rms}$$

in a noninverting amplifier design since the input impedance of this design is extremely large, the values of Rf & R1 not depend on the source impedance. Letting Rf =150 kΩ, we have

$$1 + R_f/R_1 = 2.5$$
$$R_f/R_1 = 1.5$$
$$R_1 = R_f/1.5 = (150\ \text{k}\Omega)/1.5 = 100\ \text{k}\Omega$$

The completed design is shown in Figure2-7.

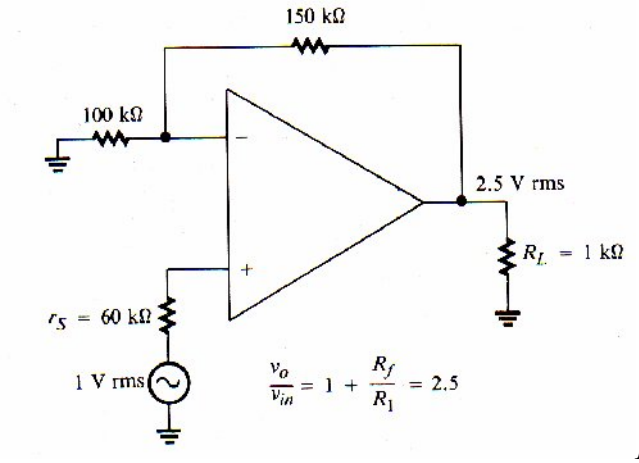
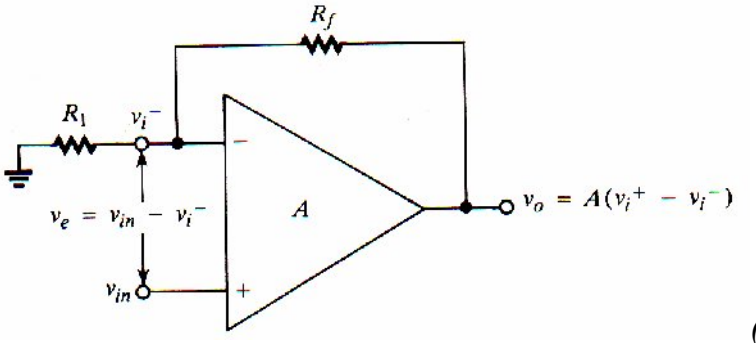


Fig 2-7 Example2-2

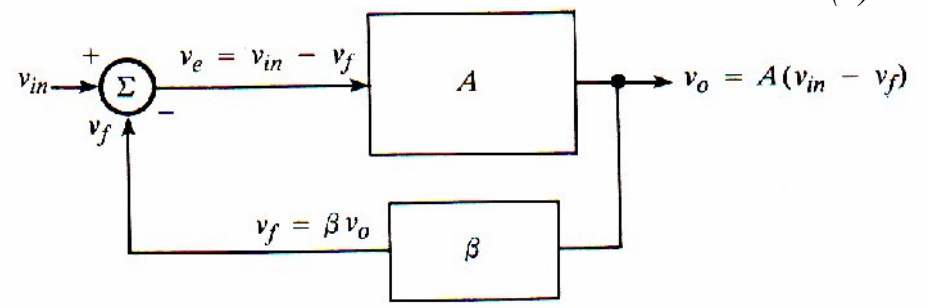
2-3 Feedback Theory

we can control the closed-loop gain vo/vin of an operational amplifier by introducing feedback through external resistor combinations.

2-3-1 feedback in the Noninverting Amplifier



(a) noninverting amplifier



(b)Block-diagram of(a)

Figure 2-8 Block-diagram representation of the noninverting amplifier. Identify corresponding voltages in the two diagrams

(A)the amplifier and its open-loop gain, (β) is called the feedback ratio and represents the output voltage that is fed back to the input. ve = vin –vf. ve is often called the error voltage. The feedback voltage vf =βvo corresponds to vi⁻ in the amplifier circuit. Since the feedback voltage subtracts from the input voltage, the amplifier is said to have negative feedback.

$$v_o = A(v_{in} - v_f)$$ ----------2-16

And

$$v_f = \beta v_o$$ ----------2-17

Substituting (2-17) into (2-16) gives

$$v_o = A(v_{in} - \beta v_o) = Av_{in} - A\beta v_o,$$

$$v_o(1+A\beta) = Av_{in}, \quad \text{Thus,}$$

$$\frac{v_o}{v_{in}} = \frac{A}{1 + A\beta} = \frac{1/\beta}{1 + 1/A\beta} \text{ ----------2-18}$$

Appling this result to the noninverting amplifier in Figure 2-8(a). Notice that Rf & R1 form a voltage divider across the output of the amplifier, so

$$v_i^- = \left(\frac{R_1}{R_1 + R_f}\right) v_o \text{ ----------2-19}$$

Since v_i^- is the voltage fed back from the output, means $v_i^- = v_f$ & $v_f = \beta v_o$, we conclude that

$$\beta = \frac{R_1}{R_1 + R_f} \quad \text{(noninverting amplifier)} \text{ ----------2-20}$$

Substituting into (2-18), we find

$$\frac{v_o}{v_{in}} = \frac{(R_1 + R_f)/R_1}{1 + 1/A\beta} = \frac{(R_1 + R_f)/R_1}{1 + (R_1 + R_f)/AR_1} \text{ ----------2-21}$$

(2-21) determine open-loop gain A in determination of the closed-loop gain vo/vin , when A = ∞, (2-21) reduces to vo/vin = (R1+Rf)/ R1 , which is exactly the same result we obtained for the ideal, non inverting amplifier (2-15). Notice also that

$$\frac{v_o}{v_{in}} = \frac{1}{\beta} \quad \text{(ideal amplifier, } A = \infty\text{)} \text{ ----------2-22}$$

Example 2-3. *Find the closed-loop gain of the amplifier in Figure 2-9 when (1)A = ∞, (2) A = 10^6, and (3) A = 10^3.*

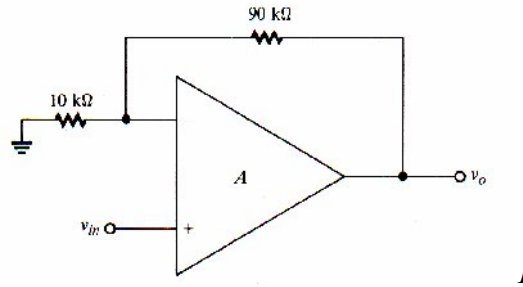


Fig 2-9 Example 2-3

Solution: *1.the feedback ratio is*

$$\beta = \frac{R_1}{R_1 + R_f} = \frac{10\ \text{k}\Omega}{(10\ \text{k}\Omega) + (90\ \text{k}\Omega)} = 0.1$$

the closed-loop gain when A = ∞ is vo/vin = 1/β = 1/0.1 = 10.

2.Using (2-18), the closed-loop gain when A = 10^6 is

$$\frac{v_o}{v_{in}} = \frac{A}{1 + A\beta} = \frac{10^6}{1 + 10^6(0.1)} = 9.99990$$

vo/vin is for all practical purposes the same value when A = 10^6 as it is when A = ∞.

3. When A = 10^3

$$\frac{v_o}{v_{in}} = \frac{10^3}{1 + 10^3(0.1)} = 9.90099$$

Problem1: *An operational amplifier has open-loop gain A = 10,000. Compare its closed-loop gain with that of an ideal amplifier when (1) β = 0.1, and (2) β= 0.001.*

In the noninverting amplifier, the input resistance seen by the signal source is

$$r_{in} = (1 + A\beta)r_{id} \approx A\beta r_{id}$$ ----------2-23

rid is the differential input resistance of the amplifier. if rid=20 kΩ, A=10^5, & β=0.01, then rin=(20 x 10^3)(10^5)(0.01)=20 MΩ, a very respectable value
The closed-loop output resistance of the noninverting amplifier is also improved by negative feedback:

$$r_o(\text{stage}) = \frac{r_o}{1 + A\beta} \approx \frac{r_o}{A\beta}$$ ----------2-24

ro is the open-loop output resistance of the amplifier. (2-24) shows the output resistance is decreased by the same factor by which the input resistance is increased. A typical value for ro is 75 Ω, so with A=10^5 & β=0.01, ro(stage)=75/10^3=0.075 Ω,

2-3-2 Feed back in the Inverting Amplifier

To investigate the effect of open-loop gain A and feedback ratio β on the closed-loop gain of the inverting amplifier, let us recall equations 2-6 and 2-7

$$\frac{v_{in}}{R_1} - \frac{v_i^-}{R_1} = \frac{v_i^-}{R_f} - \frac{v_o}{R_f}$$ ----------2-25

$$v_i^- = -v_o/A$$ ----------2-26

Substituting (2-26) into (2-25) gives

$$\frac{v_{in}}{R_1} + \frac{v_o}{AR_1} = \frac{-v_o}{AR_f} - \frac{v_o}{R_f}$$ ----------2-27

(2-27) can be solved for vo/vin with the result

$$\frac{v_o}{v_{in}} = \frac{-R_f/R_1}{1 + (R_1 + R_f)/AR_1}$$ ----------2-28

$$\frac{v_o}{v_{in}} = \frac{-R_f/R_1}{1 + 1/A\beta}$$ ----------2-29

the closed-loop gain reduces to the ideal amplifier value (-Rf/R1) when A=∞. By the superposition principle, we can analyze the contribution of the feedback source by grounding all other signal sources. When this is done, , we see that the feedback voltage in both configurations is developed across R1, Rf voltage divider,& β=R1/(R1+Rf) in both cases. , (2-28) can write as

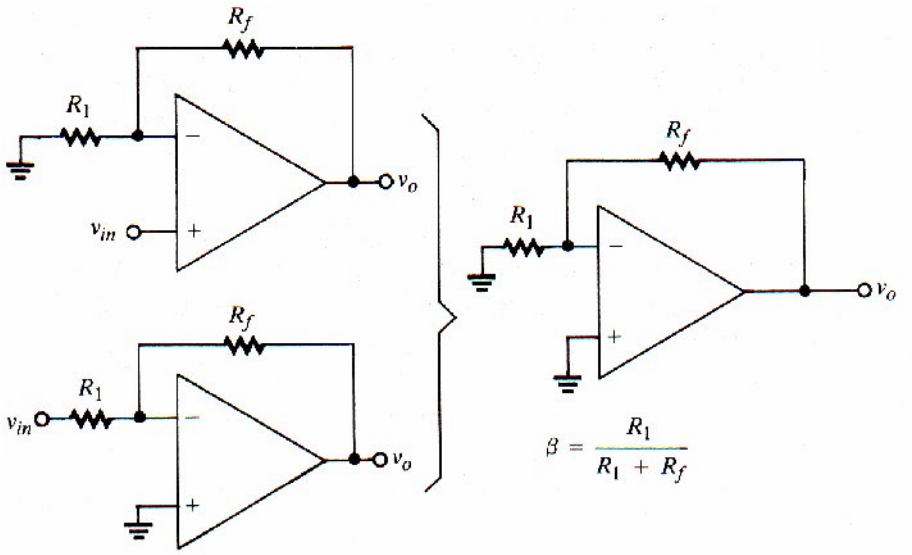


Figure 2-10 When vin is grounded in both the inverting and noninverting amplifiers, it can be seen that the feedback paths are identical

Figure 2-11 is quite similar to Figure 2-8(b) for the noninverting amplifier, except that we now denote the open loop gain by –A , v represent an arbitrary input voltage, rather than vin.

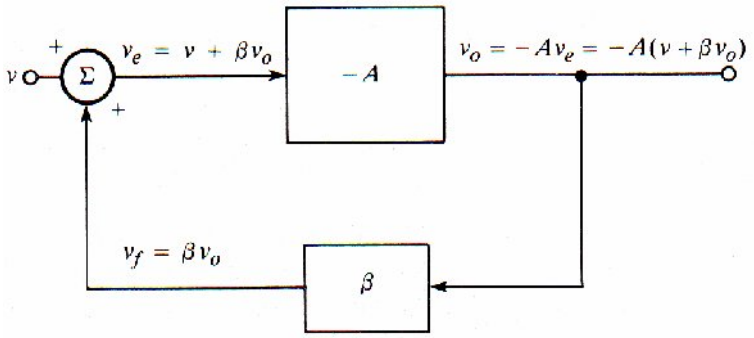


Figure 2-11 First step in the development of a feedback model for the inverting amplifier
As shown in fig2-11

$$v_o = -A(v + \beta v_o) \quad \text{----------2-30}$$

Solving for vo/v we find

$$\frac{v_o}{v} = \frac{-A}{1 + A\beta} = \frac{-1/\beta}{1 + 1/A\beta} \quad \text{----------2-31}$$

(2-31) for the model can be written

$$\frac{v_o}{v} = \frac{\frac{-(R_1 + R_f)}{R_1}}{1 + 1/A\beta} \quad \text{----------2-32}$$

If the right side of (2-32) were multiplied by the factor Rf/(R1+ Rf), we would obtain

$$\frac{v_o}{v} = \left[\frac{-(R_1 + R_f)}{\dfrac{R_1}{1 + 1/A\beta}}\right]\frac{R_f}{(R_1 + R_f)} = \frac{-R_f/R_1}{1 + 1/A\beta} \quad \text{----------2-33}$$

(2-33) gives us exactly the same result (2-29 with vin = v) that we obtain for the inverting amplifier. Therefore, we modify the block-diagram model in Figure 2-11 by adding a block that multiplies the input by Rf/(R1+Rf). The complete feedback model is shown in Figure 2-12, shown that the loop gain for the inverting amplifier is Aβ, the same as that for the noninverting amplifier

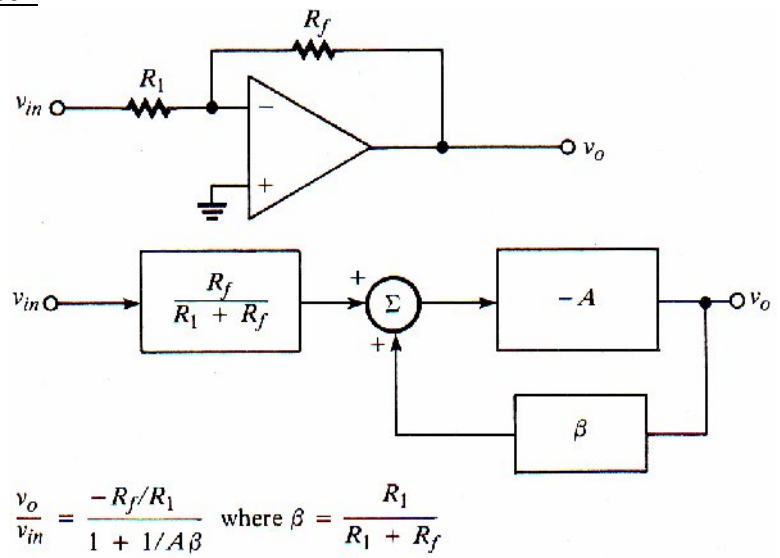


Figure2-12 The complete feedback model for the inverting amplifier

$$r_{in} = R_1 + \frac{R_f}{1 + A} \approx R_1 \quad \text{----------2-34}$$

$$r_o(\text{stage}) = \frac{r_o}{1 + A\beta} \approx \frac{r_o}{A\beta} \quad \text{----------2-35}$$

Example 2-5. *The amplifier shown in Figure 2-13 has open-loop gain equal to -2500 and open-loop output resistance100Ω. Find*

1. the magnitude of the loop gain,
2. the closed-loop gain,
3. the input resistance seen by vin, and
4. the closed-loop output resistance.

Solution:*1.*

$$\beta = R_1/(R_1 + R_f) = (1.5\ \text{k}\Omega)/[(1.5\ \text{k}\Omega) + (150\ \text{k}\Omega)] = 9.90099 \times 10^{-3}$$

Loop gain

$$= A\beta = (2.5 \times 10^3)(9.90099 \times 10^{-3}) = 24.75$$

2.From Equation 2-29

$$\frac{v_o}{v_{in}} = \frac{-R_f/R_1}{1 + 1/A\beta} = \frac{-(150\ \text{k}\Omega)/(1.5\ \text{k}\Omega)}{1 + 1/24.75} = -96.12$$

3.From equation 2-34

$$r_{in} = R_1 + \frac{R_f}{1 + A} = (1.5\ \text{k}\Omega) + \frac{150\ \Omega}{1 + 2500} = 1560\ \Omega$$

4.From Equation 2-35

$$r_o(\text{stage}) = \frac{r_o}{1 + A\beta} = \frac{100}{1 + 24.75} = 3.88\ \Omega$$

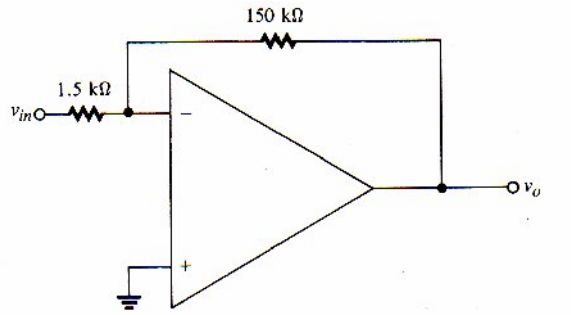


Figure 2-13 Example2-5

*the **same** relationship between actual and ideal closed-loop gain applies to inverting and noninverting amplifiers. This relationship is*

$$\text{actual } \frac{v_o}{v_{in}} = \frac{(\text{ideal closed–loop gain})}{1 + 1/A\beta} \quad \text{----------2-36}$$

ideal closed-loop gain is the closed-loop gain vo/vin result if the amplifier ideal.

$$\frac{v_o}{v_{in}} = \frac{(R_1 + R_f)/R_1}{1 + 1/A\beta} \quad \text{(noninverting amplifier)}$$

$$\frac{v_o}{v_{in}} = \frac{-R_f/R_1}{1 + 1/A\beta} \quad \text{(inverting amplifier)}$$

the greater the loop gain Aβ, the closer the closed-loop gain to the ideal closed-loop gain.

2-4 Frequency Response

2-4-1 Stability

When stability is used in high-gain amplifier, it means behaving like an amplifier rather than like an oscillator. an operational amplifier has very high gain, so precautions must be taken in its design to ensure that it does not oscillate(an oscillator is a device that generates an ac signal because of positive feedback), large gains at high frequencies tend to make an amplifier unstable, to ensure stable operation, most operational amplifiers have internal compensation circuitry that causes the open-loop gain to diminish with increasing frequency. This reduction in gain is called rolling-off the amplifier. The usable frequency range rolls off at the rate of -20 dB/decade, or -6 dB/octave.

2-4-2 The Gain-Bandwidth Product

Figure 2-14 shows frequency response characteristic for the open-loop gain of an operational amplifier, fc is the cutoff frequency(the frequency at which the gain A falls to √2/2 times its low-frequency or dc value A_0), the slope of the single-pole response is -1.
the frequency at which the β falls to the value 1 is given by $f_T = \beta_m f_\beta$
where β_m is the low frequency β & f_B is the β cutoff frequency

$$f_t = A_0 f_c \quad \text{----------2-37}$$

Where f_t = the unity-gain frequency, the frequency at which the gain equals 1
A_0= the low-frequency, or dc, value of the open-loop gain

f_c = the cutoff frequency, or 3-dB frequency, of the open-loop gain
$A_0 f_c$ the gain-bandwidth product because the bandwidthBW = f_c =0 since the Amplifier is dc

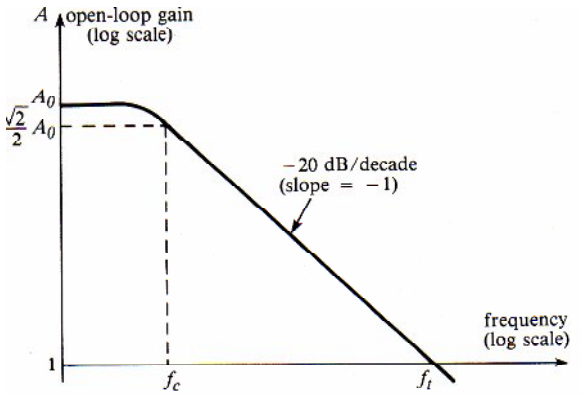


Figure 2-14 Frequency response of the open-loop gain of an operational amplifier. A_0 = dc gain, f_c = cutoff frequency, f_t = unity-gain frequency

the closed-loop bandwidth BW_{CL} and the gain-bandwidth product is closely approximated by

$$BW_{CL} = f_t\beta = A_0 f_c \beta \quad \text{----------2-38}$$

the fact that the ideal closed-loop gain is 1/β makes equation 2-38 equivalent to

$$BW_{CL} = f_t/(\text{ideal closed-loop gain}) \quad \text{----------2-39}$$

or (ideal closed-loop gain) x (closed-loop bandwidth) = gain-bandwidth product.

***Example 2-6**. Each of the amplifiers shown in Figure 2-15 has an open-loop, gain bandwidth product($A_0 f_c$) equal to 1 x 10^6. Find the cutoff frequencies(f_c)in the closed-loop configurations shown.*

Solution.

***1.**In Figure 2-15(a), $\beta=R1/(R1+R_f)=(10\ k\Omega)/[(10\ k\Omega)+(240\ k\Omega)]=0.04$.*
From equation 2-38, $BW_{CL}=f_t\beta=(10^6)(0.04)=40$ kHz.
Since the amplifier is dc, the closed-loop f_c is the same as the closed-loop bandwidth, 40 kHz.
***2.**In Figure 2-15(b), $\beta=R1/(R1+Rf)=(10k\Omega)/[(10k\Omega)+(15k\Omega)]=0.4$.*
Then $BWCL=10^6(0.4)=400$ kHz.
***1**. the ideal closed-loop gain is $(R1+Rf)/R1=(250\ k\Omega)/(10\ k\Omega)=25$*
So 25 x (closed-loop bandwidth) = 10^6, which yields
closed-loop bandwidth = BW_{CL} = 40 kHz (correct)
***2.** we have ideal closed-loop gain=$Rf/R1=(15\ k\Omega)/(10\ k\Omega)=1.5$*
from equation 2-39, $BW_{CL}=10^6/1.5=666.6$ kHz (incorrect)

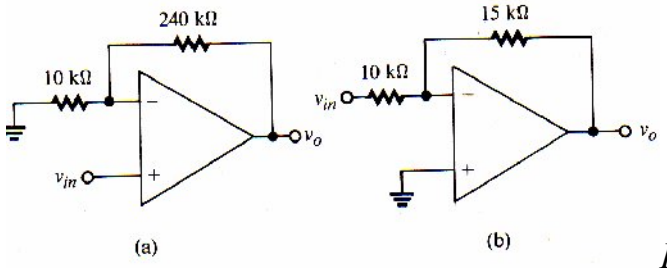


Figure 2-15 (Example 2-6)

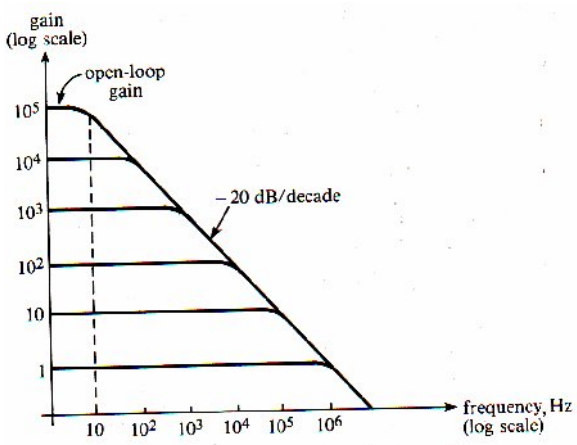


Figure 2-16 A typical set of frequency response plots for a noninverting amplifier

Figure 2-16 shows the bandwidth decreases as the closed-looped gain increases.

***Example 2-7**. for the amplifier whose frequency response is shown in figure 2-16, find*
1. the unity-gain frequency,
2. the gain-bandwidth product,
3. the bandwidth when the feedback ratio is 0.02, and
4. the closed-loop gain at 0.4 MHz when the feedback ratio(β) is 0.04.
Solution.
1. In Figure 2-16, seen the open-loop gain=1 when the frequency is 1MHz. Thus, f_t=1 MHz.
2. Gain-bandwidth product = $A_0 f_c = f_t = 10^6$.
3. From equation 2-38, $BW_{cL} = f_t\beta = 10^6(0.02) = 20$ kHz.
4. $BW_{CL}=f_t\beta=10^6(0.04)=40$ kHz. Thus, the closed-loop cutoff frequency is 40 kHz.
Since the amplifier is noninverting, the closed-loop gain is 1/β=25. Since 0.4 MHz is1 decade above the cutoff frequency, the gain is down 20 dB from 25,

2-4-3 Slew Rate
The internal compensation circuitry used to ensure amplifier stability also affects the frequency response and places a limit on the maximum operating frequency. The capacitor(s) in this compensation circuitry limit amplifier performance because when the amplifier is driven by pulse-type signal, the capacitance must charge and discharge rapidly in order for the output to keep up with the input. Since the voltage across a capacitor cannot be changed instantaneously, there is an inherent limit on the rate at which the output voltage can change.
The maximum possible rate at which an amplifier's output voltage can change, in volts per second, is called its slew rate.

$$\text{rate of change} = \frac{V_2 - V_1}{t_2 - t_1} = \frac{\Delta V}{\Delta t} \text{ volts/second} \qquad \text{----------2-40}$$

Since the slew rate of an amplifier is the maximum rate at which its output can change, we cannot drive the amplifier with any kind of input waveform that would require the output to exceed that rate.

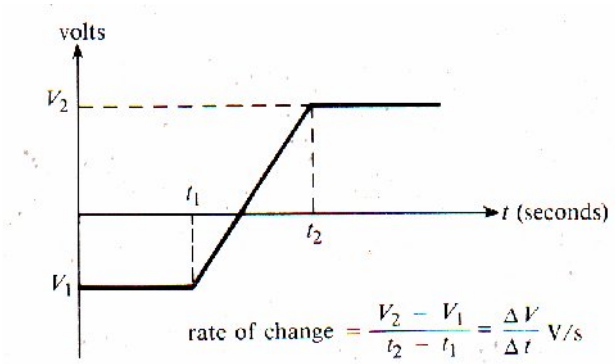


Figure 2-17 The rate of change of a linear, or ramp, signal is the change in voltage divided by the change in time.

Example 2-8. *The operational amplifier in Figure 2-18 has a slew rate specification of 0.5 V/μs. If the input is the ramp waveform shown, what is the maximum closed-loop gain that the amplifier can have without exceeding its slew rate?*

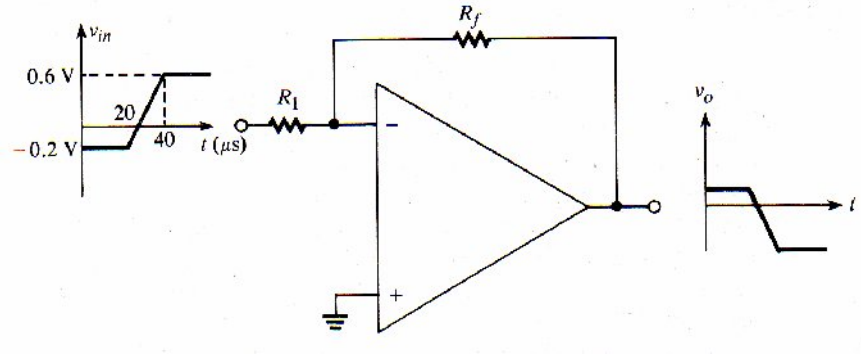


Figure 2-18 (Example 2-8)

Solution.

The rate of change of the input is

$$\frac{\Delta V}{\Delta t} = \frac{V_2 - V_1}{t_2 - t_1} = \frac{0.6 - (-0.2)}{(40 - 20) \times 10^{-6}} = 4 \times 10^4 \text{ V/s}$$

Since the slew rate is 0.5 V/μs = 5 X 10^5 V/s, the maximum permissible gain is

$$\frac{5 \times 10^5 \text{ V}}{4 \times 10^4 \text{ V}} = 12.5$$

the amplifier is inverting configuration, so the output changes from positive to negative. the gain is -12.5, the output change from (-12.5)(-0.2)= +2.5V to (-12.5)(0.6) = -7.5V in 20μs. (+2.5V – (-7.5V))/20μs = 10V / 20μs = 0.5 V/μs.

$$\frac{\Delta V}{\Delta t} = \frac{10 \text{ V}}{20 \text{ μs}} = 0.5 \text{ V/μs}$$

the maximum frequency at which An amplifier can be operated depends on both the bandwidth and the slew rate.

2-5 Offset Current &Voltages

one of the characteristics of an ideal operational amplifier is that it has zero output voltage when both inputs are 0 volts (grounded). The actual value of the output voltage when the inputs are 0 is called the ***output offset voltage****. Output offset is very much like a dc bias level*

in the output of a conventional amplifier, in that it is added to whatever signal variation occurs there.
Manufacturers do not generally specify output offset because, the offset level depends on the closed-loop gain that a user designs through choice of external component values. Instead, input offsets are specified, and the designer can use these values to compute the output offset that results in a particular application. Output offset voltages are the result of two distinct input phenomena: 1- input bias currents and 2- input offset voltage.

2-5-1 Input Offset Current

We know that some dc base current must flow when a transistor is properly biased, although its small its flowing through the external resistors produces a dc input voltage that in turn creates an output offset. To reduce the effect of bias currents, Rc is connected in series with the non inverting (+) terminal of the amplifier (Rc provide a dc path to ground, so if a signal is capacitor coupled to the + input, Rc must be connected between the + input and ground.) proper choice of the value of Rc will minimize the output offset voltage due to bias current.

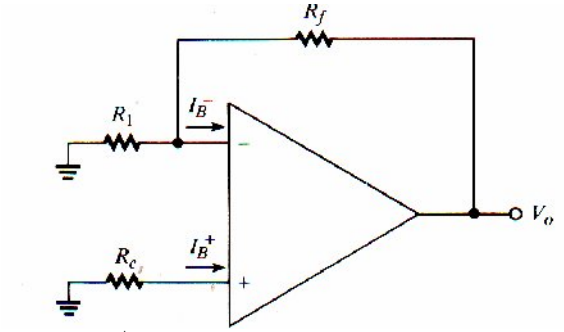


Figure 2-23 Input bias currents I_B^+ and I_B^- that flow when both signal inputs are grounded. Rc is a compensating resistor used to reduce the effect of bias current on output offset.

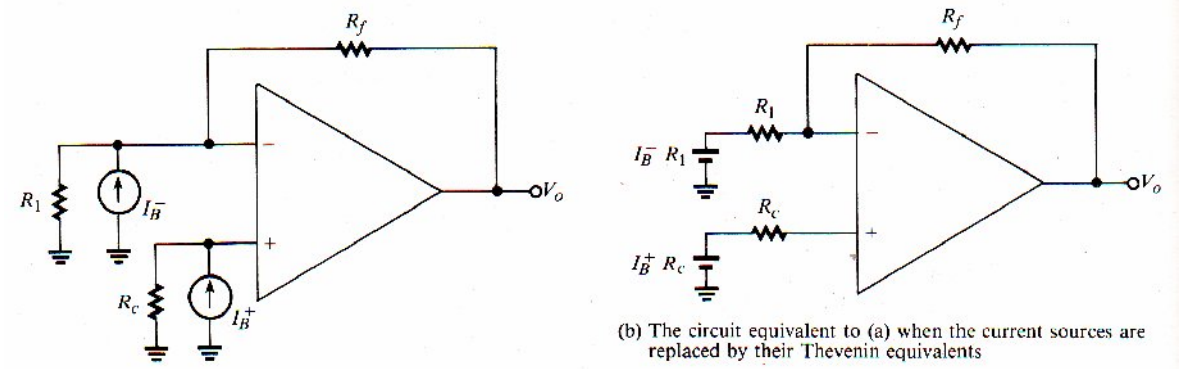


Figure 2-24 Circuits equivalent to Figure 2-23

We can apply the superposition principle to determine the output offset voltage due to each input source acting alone. As in Figure 2-25(a) the amplifier acts as an inverter when the source connected to the + terminal is shorted to ground, so the output due to I_B^- R1 is

$$V_{o1} = I_B^- R_1 \left(\frac{-R_f}{R_1}\right) = -I_B^- R_f$$ ----------2-51

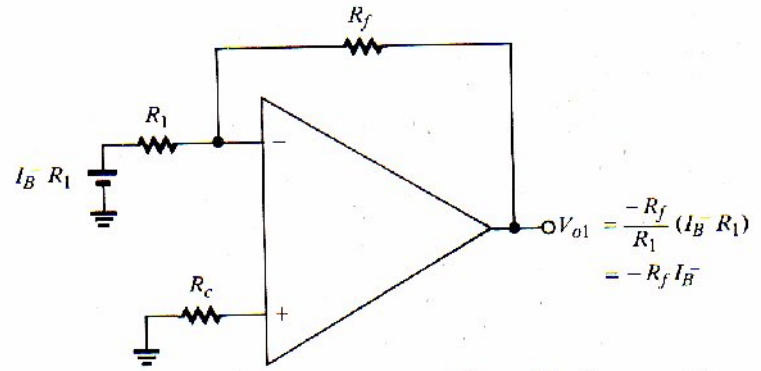
When the source connected to the - terminal is shorted to ground, the amplifier is in a non inverting configuration, so the output due to I_B^+ R1 is

$$V_{o2} = I_B^+ R_c \left(\frac{R_f + R_1}{R_1}\right) \text{----------2-52}$$

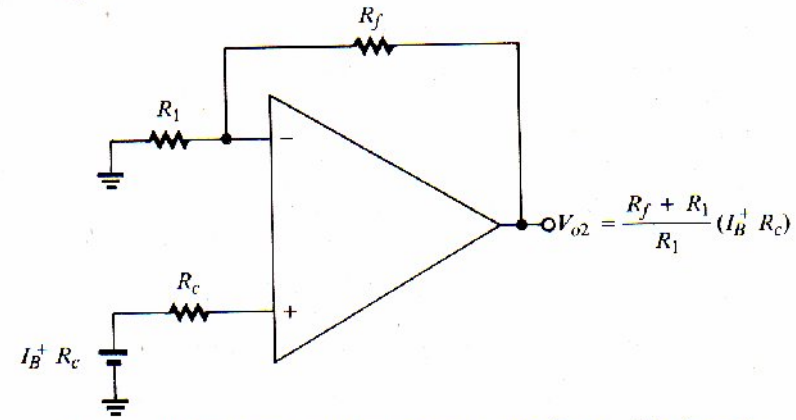
Combining (2-51) and (2-52), we obtain the total output offset voltage due to bias current, which we designate by $V_{OS}(I_B)$, as

$$V_{OS}(I_B) = I_B^+ R_c \left(\frac{R_f + R_1}{R_1}\right) - I_B^- R_f \text{----------2-53}$$

$V_{OS}(I_B)$ may be positive or negative. negative offset voltage is just as undesirable as positive offset voltage. Our real interest is in finding a way to minimize the magnitude of $V_{OS}(I_B)$.



(a) When the noninverting input is grounded, the amplifier inverts and has gain $-R_f/R_1$.



(b) When the inverting input is grounded, the noninverting amplifier has gain $(R_f + R_1)/R_1$.

Figure 2-25 Applying superposition to determine the output offset voltage due to each source in Figure 2-24(b)

let us make assumption that the two inputs are closely matched and that have equal bias currents: $I_B^+ = I_B^- = I_{BB}$. Substituting I_{BB} for I_B^- and I_B^+ in equation 2-53 gives

$$V_{OS}(I_B) = I_{BB}\left[R_c\left(\frac{R_f + R_1}{R_1}\right) - R_f\right] \text{----------2-54}$$

If the expression enclosed by the brackets in (2-54) = 0, we would have zero offset voltage. To find a value of Rc. we set the bracketed expression = 0 and solve for Rc

$$R_c\left(\frac{R_f + R_1}{R_1}\right) - R_f = 0$$

$$R_c = \frac{R_f}{\frac{R_f + R_1}{R_1}} = \frac{R_f R_1}{R_f + R_1} = R_f \parallel R_1$$

-------2-55

(2-55) reveals that output offset due to input bias currents can be minimized by connecting a resistor Rc having value R1 ‖ Rf in series with the non inverting input. We can compute the exact value of $V_{OS}(I_B)$ when Rc = R1 ‖ Rf by substituting this value of Rc back into (2-53).

$$\begin{aligned} V_{OS}(I_B) &= I_B^+(R_1 \parallel R_f)\left(\frac{R_f + R_1}{R_1}\right) - I_B^- R_f \\ &= I_B^+\left(\frac{R_1 R_f}{R_1 + R_f}\right)\left(\frac{R_f + R_1}{R_1}\right) - I_B^- R_f \\ &= (I_B^+ - I_B^-)R_f \end{aligned}$$

----------2-56

(2-56) shows the offset voltage is proportional to the difference between I_B^+ & I_B^- when Rc=R1 ‖ Rf. The equation confirms that $V_{OS} = 0$ if I_B^+ exactly equals I_B^-.
The quantity (I_B^+ - I_B^-) is the input offset current and is often quoted in manufacturers specifications. Letting the input offset current (I_B^+ - I_B^-) be I_{io}, we have, from(2-56),

$$V_{OS}(I_B) = I_{io}R_f \quad \text{when } R_c = R_1 \parallel R_f$$

----------2-57

$V_{OS}(I_B)$ may be either positive or negative, depending on whether $I_B^+ > I_B^-$ or vice versa, so a more useful form of (2-57) is

$$|V_{OS}(I_B)| = |I_{io}|R_f \quad \text{when } R_c = R_1 \parallel R_f$$

----------2-58

Manufacturers specifications always give a positive value for I_{io} (absolute value).
From (2-58) the output offset is directly proportional to Rf. For that reason, small resistance values should be used when offset is a critical consideration. Another common manufacturers specification is called input bias current I_B.By convention, I_B is the average of I_B^+ and I_B^-;

$$I_B = \frac{I_B^+ + I_B^-}{2}$$

----------2-59

I_B typically much larger than I_{io} because I_B is on the same order of magnitude as I_B^+ & I_B^-, while I_{io} is the difference between the two. Given values for I_B & I_{io}, we can find I_B^+ & I_B^-, provided we know which is the larger. If $I_B^+ > I_B^-$, then

$$\left.\begin{aligned} I_B^+ &= I_B + 0.5\,|I_{io}| \\ I_B^- &= I_B - 0.5\,|I_{io}| \end{aligned}\right\} (I_B^+ > I_B^-)$$

----------2-60

If $I_B^- > I_B^+$

$$\left.\begin{aligned} I_B^+ &= I_B - 0.5\,|I_{io}| \\ I_B^- &= I_B + 0.5\,|I_{io}| \end{aligned}\right\} (I_B^- > I_B^+)$$

----------2-61

***Example 2-13**. The specifications for the operational amplifier in Figure 2-26 state that the input bias current is 80 nA and that the input offset current is 20 nA.*

1. Find the optimum value for Rc.
2. Find the magnitude of the output offset voltage due to bias currents when Rc equals its optimum value.
3. Assuming that $I_B^+ > I_B^-$, find the magnitude of the output offset voltage when Rc = 0.

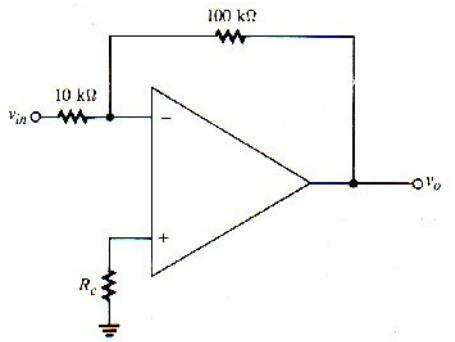


Figure 2-26 (Example 2-13)

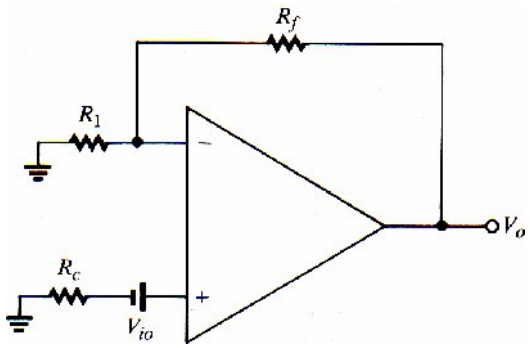


Fig 2-27 The effect of input offset voltage, Vio is the same as if a dc source were connected in series with one of the input

Solution:
1. equation 2-55, $Rc = R1 \parallel R_f = (10\ k\Omega) \parallel (100\ k\Omega) = 9.09\ k\Omega.$

2. equation 2-58, $|V_{OS}(I_B)| = |I_{io}| R_f = (20 \times 10^{-9})(100 \times 10^3) = 2\ mV.$

3. equation 2-53, When Rc = 0, $V_{OS}(I_B) = -I_B^- R_f$
equation 2-60, $I_B^- = I_B - 0.5\, I_{io} = (80\ nA) - 0.5(20\ nA) = 70\ nA.$
Therefore,
$$|V_{os}(I_B)| = (70 \times 10^{-9})(100 \times 10^3) = 7\ mV.$$

2-5-2 Input Offset Voltage
Another input phenomenon that contributes to output offset voltage is an internally generated potential difference that exists because of imperfect matching of the input transistors. This potential may be due to a difference between the VBE drops of the transistors in the input differential stage of a BJT amplifier. Called input offset voltage, the net effect of this potential difference is the same as if a small dc voltage source were connected to one of the inputs(figure 2-27). The output voltage when the input is V_{io} is given by

$$V_{OS}(V_{io}) = V_{io} \frac{(R_1 + R_f)}{R_1} \quad \text{----------2-62}$$

$V_{OS}(V_{io})$ is the output offset voltage due to V_{io} . for a wide variety of amplifier configurations, it is true that

$$V_{OS}(V_{io}) = V_{io}/\beta \quad \text{----------2-63}$$

Example 2-14*. The specifications for the amplifier in Example 2-13 state that the input offset voltage is 0.8 m V. Find the output offset due to this input offset.*
Solution*. From equation 2-62*

$$V_{OS}(V_{io}) = V_{io}\frac{(R_1 + R_f)}{R_1} = (0.8 \times 10^{-3}\ \text{V})\frac{[(10\ \text{k}\Omega) + (100\ \text{k}\Omega)]}{10\ \text{k}\Omega} = 8.8\ \text{mV}$$

2-5-3 The Total Output Voltage

We have seen that output offset voltage is a function of two distinct input characteristics: input bias currents and input offset voltage. it is good design practice to assume a worst-case situation, in which the two offsets have the same polarity and reinforce each other, for the worst-case situation, we assume that the total offset is the sum of the respective magnitudes:

$$|V_{OS}| = |V_{OS}(I_B)| + |V_{OS}(V_{io})| \quad \text{(worst case)} \qquad \text{----------2-64}$$

where V_{os} is the total output offset voltage.

***Example 2-15**. The operational amplifier in Figure 2-28 has the following specifications: input bias current =100 nA; input offset current =20 nA; input offset voltage =0.5 mV. Find the worst-case output offset voltage. (Consider the two possibilities $I_B^+ > I_B^-$ and vice versa.)*

***Solution**: We first check to see if the 10 kΩ resistor in series with the non inverting input has the optimum value of a compensating resistor: $R1 \parallel R_f = (15\ \text{k}\Omega) \parallel (75\ \text{k}\Omega) = 12.5\ \text{k}\Omega$.*

$Rc = 10\ \text{k}\Omega$ is not optimum, and we will have to use equation 2-53 to find $V_{OS}(I_B)$. Assuming first that In $I_B^+ > I_B^-$, we have, from equation 2-60,

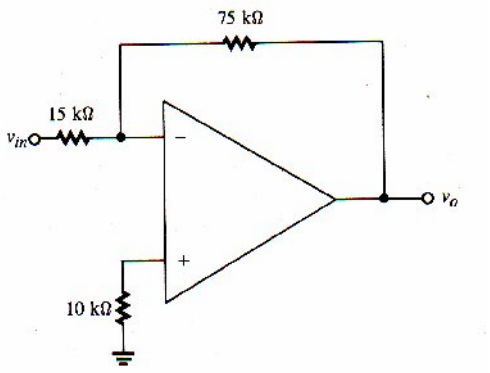


Figure 2-28 (Example 2-15)

$$I_B^+ = I_B + 0.5I_{io} = (100\ \text{nA}) + 0.5(20\ \text{nA}) = 110\ \text{nA}$$
$$I_B^- = I_B - 0.5I_{io} = (100\ \text{nA}) - 0.5(20\ \text{nA}) = 90\ \text{nA}$$

Therefore, by equation 2-53,

$$V_{OS}(I_B) = I_B^+ R_c\left(\frac{R_f + R_1}{R_1}\right) - I_B^- R_f$$
$$= (110 \times 10^{-9})(10 \times 10^3)\left(\frac{75 \times 10^3 + 15 \times 10^3}{15 \times 10^3}\right) - (90 \times 10^{-9})(75 \times 10^3)$$
$$= -0.15\ \text{mV}$$

If $I_B^- > I_B^+$, then $I_B^+ = 90$ nA and $I_B^- = 110$ nA. In that case,

$$V_{OS}(I_B) = (90 \times 10^{-9})(10 \times 10^3)\left(\frac{75 \times 10^3 + 15 \times 10^3}{15. \times 10^3}\right) - (110 \times 10^{-9})(75 \times 10^3)$$
$$= -2.85\ \text{mV}$$

the worst case occurs for $I_B^- > I_B^+$, therefore assume that $|V_{OS}(I_B)|$ =2.85 mV. By (2-62)

$$V_{OS}(V_{io}) = \frac{V_{io}(R_1 + R_f)}{R_1} = (0.5\text{ mV})\left[\frac{(15\text{ k}\Omega) + (75\text{ k}\Omega)}{15\text{ k}\Omega}\right] = 3\text{ mV}$$

the worst case offset is $V_{OS}=|V_{OS}(I_B)|+|V_{OS}(V_{io})|$ =(2.85mV)+(3mV)=5.85mV. (the best case offset would be 0.15mV)

***Example 2-16**. Assuming worst-case conditions at 25°C, determine the following, in connection with the μA741 operational-amplifier circuit shown in Figure 2-30. in the 741 specifications list the unity-gain frequency to be 1 MHz , the maximum value of input offset current(Iio) to be 200nA , the maximum value of input offset voltage(Vio) to be 5 m V .find*
1. the closed-loop bandwidth,
2. the total output offset voltage $|V_{OS}|$
Solution.
1. From equation 2-38, $BW_{CL} = f_t\beta$. From Figure 2-30,

$$\beta = \frac{R_1}{R_1 + R_f} = \frac{12\text{ k}\Omega}{(12\text{ k}\Omega) + (138\text{ k}\Omega)} = 0.08$$

$$\text{Thus, } BW_{CL} = (1\text{ MHz})(0.08) = 80\text{ kHz}.$$

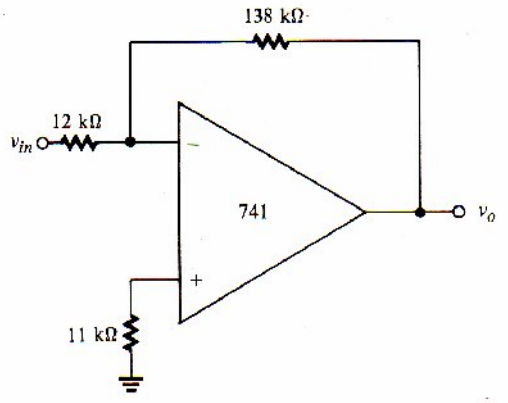


Figure 2-30 (Example 2-16)

2. $R1 \| R_f = (12\text{ k}\Omega) \| (138\text{ k}\Omega) = 11\text{ k}\Omega$.

the compensating resistor has its optimum value and we can use(2-58) to determine the output offset due to bias currents: $|V_{OS}(I_B)| = |Iio| R_f$
Therefore,

$$|V_{OS}(I_B)|_{max} = (200 \times 10^{-9})(138 \times 10^3) = 27.6\text{ mV}.$$

$$|V_{OS}(V_{io})| = V_{io}\left(\frac{R_f + R_1}{R_1}\right) = (5\text{ mV})\left[\frac{(138\text{ k}\Omega) + (12\text{ k}\Omega)}{12\text{ k}\Omega}\right] = 62.5\text{ mV}$$

$$\text{Finally, } |V_{OS}|_{worst\ case} = (27.6\text{ mV}) + (62.5\text{ mV}) = 90.1\text{ mV}.$$

3-Application of Operational Amplifiers

3-1Voltage Summation

It is possible to scale a signal voltage to multiply it by a fixed constant through an appropriate choice of external resistors that determine the closed-loop gain of an amplifier circuit. This operation can be accomplished in either an inverting or non inverting configuration. It is also possible to sum several signal voltages in one operational-amplifier circuit and at the same time scale each by a different factor, This called a linear combination and the circuit that produces it is often called a linear-combination circuit (Figure 3-1).

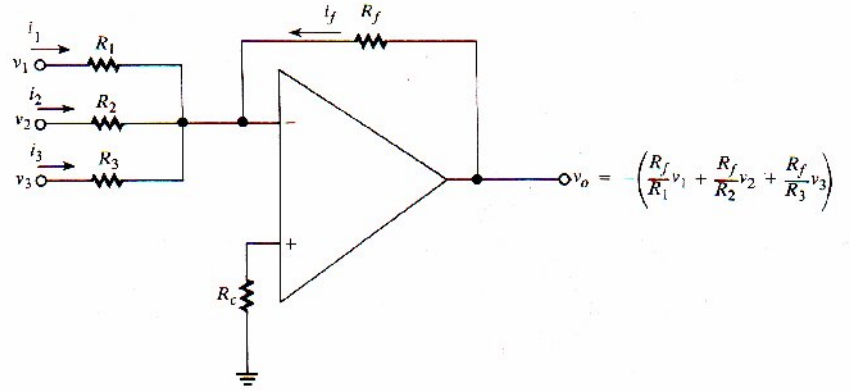


Figure 3-1 An operational-amplifier circuit that produces an output equal to the (inverted) sum of three separately scaled input signals

$$i_1 + i_2 + i_3 = i_f \text{----------3-1}$$

Or, since the voltage at the summing junction is ideally 0

$$\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3} = \frac{-v_0}{R_f} \text{ ----------3-2}$$

$$v_0 = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \frac{R_f}{R_3}v_3\right) \text{----------3-3}$$

Choose $R_1 = R_2 = R_3 = R$, then we obtain

$$v_0 = \frac{-R_f}{R}(v_1 + v_2 + v_3) \text{----------3-4}$$

for $R_f = R$

$$v_0 = -(v_1 + v_2 + v_3) \text{----------3-5}$$

The feedback ratio for the circuit is

$$\beta = \frac{R_p}{R_p + R_f} \text{----------3-6}$$

$R_p = R_1 \| R_2 \| R_3$. Using this value of β, to apply closed-loop bandwidth and output offset V_{OS}(Vin). The optimum value of the bias-current compensation resistor is

$$R_c = R_f \| R_p = R_f \| R_1 \| R_2 \| R_3 \text{----------3-7}$$

Example 3-1.

1. *Design an operational-amplifier circuit that will produce an output = $-(4v_1 + v_2 + 0.1v_3)$*

2. *Write an expression for the output and sketch its waveform when $v_1 = 2$ sin wt, $v_2 = +5$ V dc, and $v_3 = -100$ V dc*

Solution.1.*We arbitrarily choose $R_f = 60$ kΩ. Then*

$R_f/R_1 = 4 \Rightarrow R_1 = (60\ \text{k}\Omega)/4 = 15\ \text{k}\Omega$
$R_f/R_2 = 1 \Rightarrow R_2 = (60\ \text{k}\Omega)/1 = 60\ \text{k}\Omega$
$R_f/R_3 = 0.1 \Rightarrow R_3 = (60\ \text{k}\Omega)/0.1 = 600\ \text{k}\Omega$

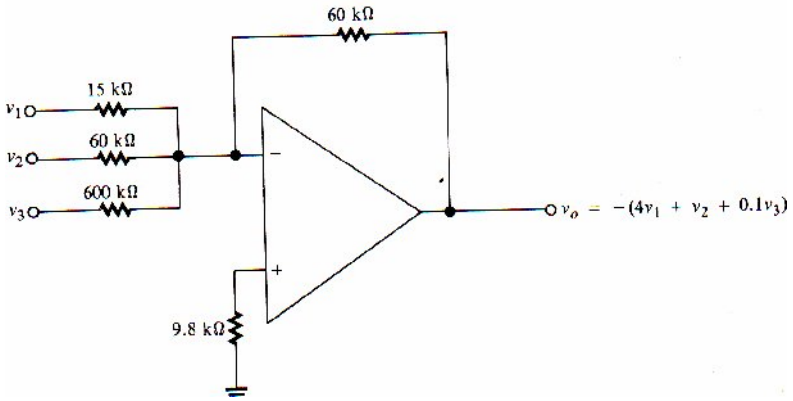


Figure 3-2 (Example 3-1)

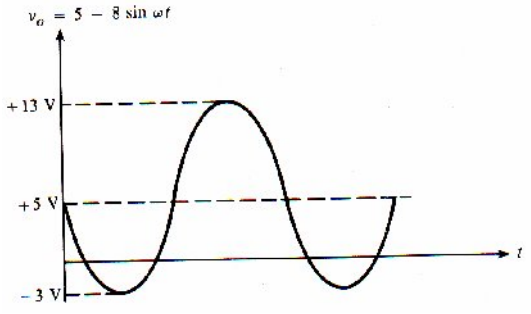


Figure 3-3 (Example 3-1)

$Rc = R_f \parallel R_1 \parallel R_2 \parallel R_3 = (60\ k\Omega) \parallel (15\ k\ \Omega) \parallel (60\ k\Omega) \parallel (600\ k\Omega) = 9.8\ k\Omega.$

2. *vo = -[4(2sin wt)+1(5)+0.1(-100)]= -8 sin wt - 5+10=5 - 8sin wt.*
Vo is sinusoidal with a 5V offset varies between 5 - 8= - 3V & 5 + 8 = 13V. Fig 3-3.

Figure 3-4 shows a noninverting version of the linear-combination circuit. In this example, only two inputs are connected and it can be shown that

$$v_o = \frac{R_g + R_f}{R_g}\left(\frac{R_2}{R_1 + R_2} v_1 + \frac{R_1}{R_1 + R_2} v_2\right) \text{----------3-8}$$

this circuit is more cumbersome than the inverting circuit, in applications where a noninverted sum is required, it can be obtained using the inverting circuit of Fig 3-1, followed by a unity-gain inverter.

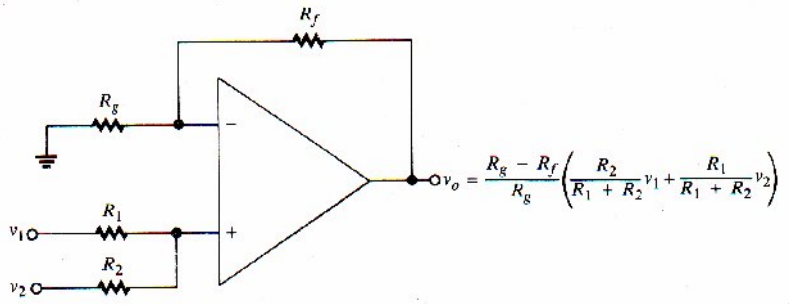


Fig 3-4 A noninverting combination

3-2 Voltage Subtraction

Produce an output voltage that equals the mathematical difference between two input signals can be performed by using the amplifier in differential mode, Fig 3-5. First, assume that v_2 is shorted to ground. Then

$$v^+ = \frac{R_2}{R_1 + R_2} v_1 \text{----------3-9}$$

$$v_{o1} = \frac{R_3 + R_4}{R_3} v^+ = \left(\frac{R_3 + R_4}{R_3}\right)\left(\frac{R_2}{R_1 + R_2}\right) v_1 \text{----------3-10}$$

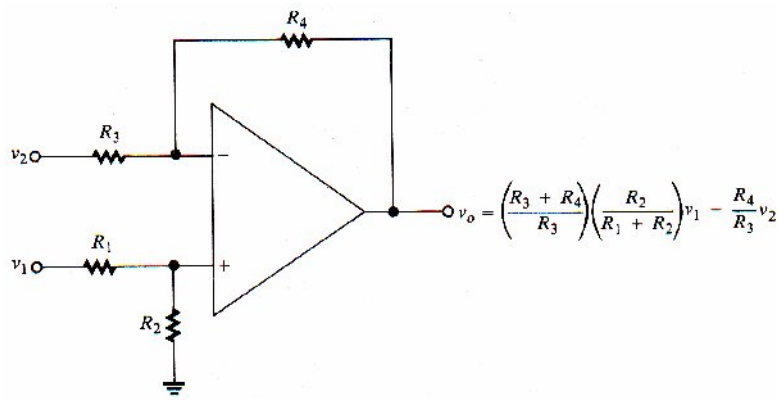


Figure 3-5 Using the amplifier in a differential mode to obtain an output proportional to the difference between two scaled inputs

Assuming now that v_1 is shorted to ground, we have

$$v_{o2} = \frac{-R_4}{R_3} v_2 \text{----------3-11}$$

$$v_o = v_{o1} + v_{o2} = \left(\frac{R_3 + R_4}{R_3}\right)\left(\frac{R_2}{R_1 + R_2}\right)v_1 - \left(\frac{R_4}{R_3}\right)v_2 \text{----------3-12}$$

Let $R_1 = R_3 = R$ and $R_2 = R_4 = AR$

Substituting these values into (3-12) gives

$$\left(\frac{R + AR}{R}\right)\left(\frac{AR}{R + AR}\right)v_1 - \frac{AR}{R} v_2 = \frac{AR}{R} v_1 - \frac{AR}{R} v_2 = A(v_1 - v_2)$$

$$v_o = A(v_1 - v_2) \text{----------3-13}$$

A is a fixed constant,($R_1 \| R_2$) is automatically the correct value ($R_3 \| R_4$), namely $R \| AR$.

Let

$$a_1 = \left(1 + \frac{R_4}{R_3}\right)\left(\frac{R_2}{R_1 + R_2}\right) \text{----------3-14}$$

$$a_2 = R_4/R_3 \text{----------3-15}$$

the output of Figure 3-5 will be

$$v_o = a_1 v_1 - a_2 v_2 \text{----------3-16}$$

$$a_1 = (1 + a_2)\frac{R_2}{R_1 + R_2} \text{----------3-17}$$

$\left(\frac{R_2}{R_1 + R_2}\right)$ *is always less than 1. Therefore to produce vo = a_1v_1 - a_2v_2 we must have*

$$(1 + a_2) > a_1 \text{----------3-18}$$

we can impose the additional condition $R_1 \| R_2 = R_3 \| R_4$. With vo = a_1v_1 - a_2v_2. ($R_1 \| R_2$) is optimum when the resistor values are selected in accordance with

$$R_4 = a_1R_1 = a_2R_3 = R_2(1 + a_2 - a_1) \text{----------3-19}$$

Example 3-2. *Design an operational-amplifier circuit with the output vo = $0.5v_1 - 2v_2$.*
Solution. *a_1=0.5 & a_2=2, so $1+a_2 > a_1$. Therefore, it is possible to construct a circuit in the configuration of Figure 3-5. we must have*

$$\left(1 + \frac{R_4}{R_3}\right)\left(\frac{R_2}{R_1 + R_2}\right) = 0.5$$

$$\frac{R_4}{R_3} = 2$$

Let us arbitrarily choose $R_4 = 100\ k\Omega$. Then $R_3 = R_4/2 = 50\ k\Omega$. Thus

$$\left(1 + \frac{R_4}{R_3}\right)\left(\frac{R_2}{R_1 + R_2}\right) = \frac{3R_2}{R_1 + R_2} = 0.5$$

choosing $R_2 = 20\ k\Omega$, we have

$$\frac{3(20\ k\Omega)}{R_1 + (20\ k\Omega)} = 0.5$$

$$60\ k\Omega = 0.5R_1 + (10\ k\Omega)$$

$$R_1 = 100\ k\Omega$$

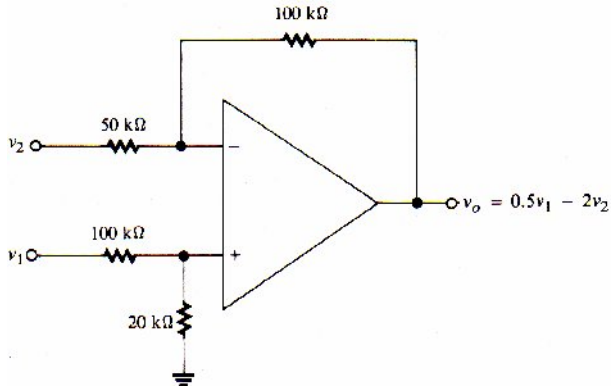


Figure 3-6 (Example 3-2)

$(R_1 \| R_2 = (100) \| (20) = 16.67k\Omega) \neq (R_3 \| R_4 = (50) \| (100) = 33.33k\Omega)$.

To apply another design , choose R_4 and solve for R_1, R_2, & R_3.
In Example 3-2, $a_1 = 0.5$ & $a_2 = 2$.
choose $R_4 = 100k\Omega$, then $R_1 = (100)/0.5 = 200k\Omega$, $R_2 = (100)/2.5 = 40k\Omega$, & $R_3 = (100)/2 = 50k\Omega$.
These choices give $R_1 \| R_2 = 33.3k\Omega = R_3 \| R_4$.
Circuit of Fig 3-5 is a useful and economic way to obtain a difference voltage of the form $A(v_1 - v_2)$, but it has limitations and complications when we want to produce an output of the general form $vo = a_1v_1 - a_2v_2$.

An alternate way to obtain a scaled difference between two signal inputs is to use two inverting amplifiers, as shown in Fig 3-7.

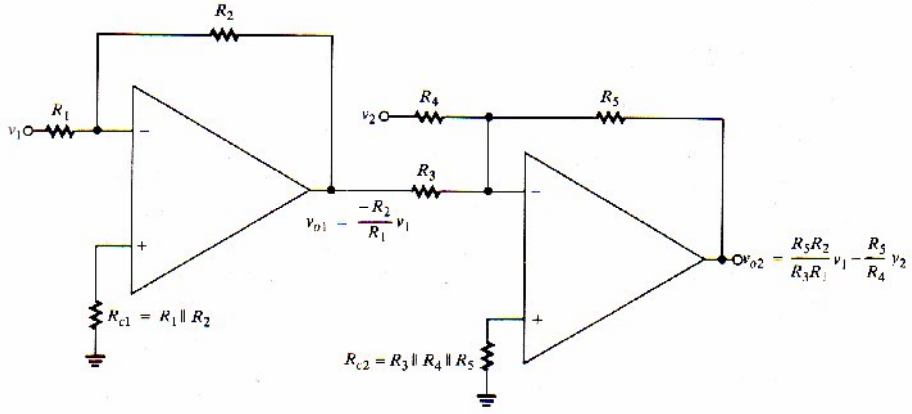


Figure 3-7 Using two inverting amplifiers to obtain the output $vo = a_1v_1 - a_2v_2$

The output of the first amplifier is

$$v_{o1} = \frac{-R_2}{R_1} v_1 \text{----------3-20}$$

and the output of the second amplifier is

$$v_{o2} = -\left(\frac{R_5}{R_3} v_{o1} + \frac{R_5}{R_4} v_2\right) = \frac{R_5 R_2}{R_3 R_1} v_1 - \frac{R_5}{R_4} v_2 \text{----------3-21}$$

$$\frac{R_5 R_2}{R_3 R_1} = a_1 \quad \text{and} \quad \frac{R_5}{R_4} = a_2 \text{----------3-22}$$

Example 3-3. *Design an operational-amplifier circuit using two inverting configurations to produce* $vo=20v_1 - 0.2v_2$.

$1+a_2=1.2 < 20=a_1$, *so we cannot use the differential circuit of Fig 3-5.*

Solution. *we can begin the process by designing the first amplifier to produce* $-20v_1$ *Choose* $R_1=10k\Omega$ *&* $R_2=200k\Omega$. *Then, the second amplifier need only invert* $-20v_1$ *with unity gain and scale the* v_2 *input by 0.2. Choose* $R_5=20k\Omega$. *Then* $R_5/R_3=1 \rightarrow R_3=20\ k\Omega$ *&* $R_5/R_4=0.2 \rightarrow R_4=100k\Omega$.*The completed design shown in Fig3-8(a). Fig3-8(b) shows another solution, in which the first amplifier produces* $-10v_1$ *and the second multiplies by the constant -2.*

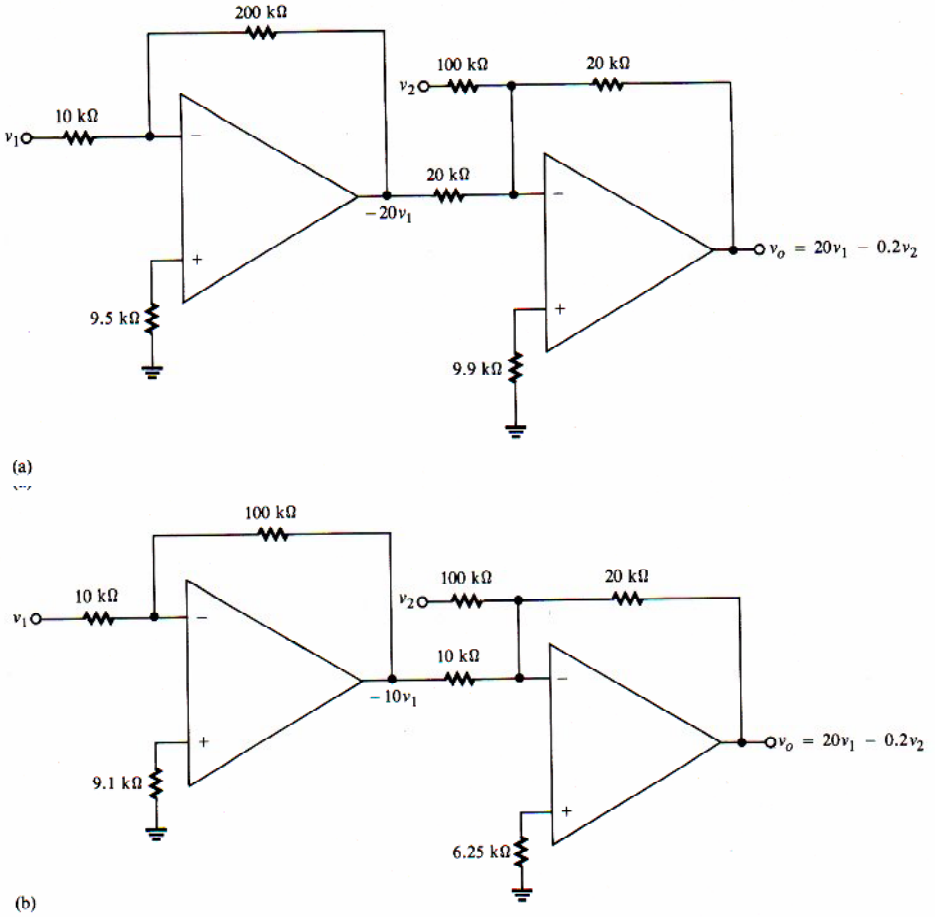


Figure 3-8 (Ex 3-3) Two (of many) equivalent methods for producing $20v_1 - 0.2v_2$ *using two inverting amplifiers*

The most general form of a linear combination is

$$vo = \pm a_1 v_1 \pm a_2 v_2 \pm a_3 v_3 \pm \ldots\ldots \pm a_n v_n .$$

Example 3-4.

1. Design an operational-amplifier circuit using two inverting configurations to produce the output $vo = -10v_1 + 5v_2 + 0.5v_3 - 20v_4$.

2. Assuming that the unity-gain frequency of each amplifier is 1MHz, find the approximate, overall, closed-loop bandwidth of your solution

***Solution.1**. Since v_2 and v_3 appear with positive signs in the output, those two inputs must be connected to the first inverting amplifier. We can produce $-(5v_2 + 0.5v_3)$ at the output of the first inverting amplifier and then invert and add it to $-(10v_1 + 20v_4)$ in the second amplifier. One possible solution is shown in Fig 3-9.*

***2.** The feedback ratio of the first amplifier is*

$$\beta_1 = \frac{(20\ \text{k}\Omega) \parallel (200\ \text{k}\Omega)}{(20\ \text{k}\Omega) \parallel (200\ \text{k}\Omega) + (100\ \text{k}\Omega)} = 0.1538$$

So $BW_{CL1} = \beta_1 f_1 = (0.1538)(1\ \text{MHz}) = 153.8$ kHz. Similarly,

$$\beta_2 = \frac{(10\ \text{k}\Omega) \parallel (100\ \text{k}\Omega) \parallel (5\ \text{k}\Omega)}{(10\ \text{k}\Omega) \parallel (100\ \text{k}\Omega) \parallel (5\ \text{k}\Omega) + (100\ \text{k}\Omega)} = 0.0312$$

and $BW_{CL2} = \beta_2 f_2 = (0.0312)(1\ \text{MHz}) = 31.2$kHz. The overall bandwidth is approximately equal to the smaller of BW_{CL1} & BW_{CL2} or 31.2 kHz

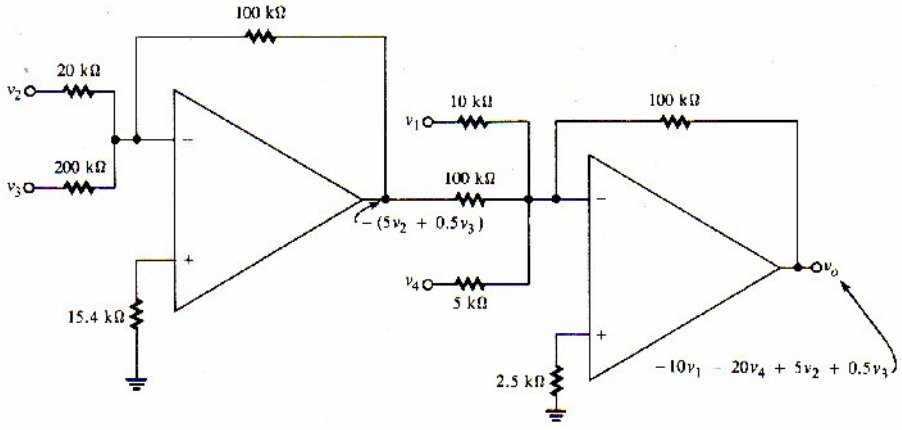


Figure 3-9 (Ex 3-4)

3-3 Controlled Voltage & Current Sources

A controlled source is one whose output voltage or current is determined by the magnitude of another, independent voltage or current.

3-3-1 Voltage-Controlled Voltage Source

An ideal, voltage-controlled voltage source (VCVS) is one whose output voltage $V_o = kV_i$ is independent of the current drawn from it.

k is dimensionless. inverting and noninverting configurations of an ideal operational amplifier meet the two criteria. since the output resistance is (ideally) 0, V_o is independent of load.

3-3-2Voltage-Controlled Current Source

An ideal, voltage-controlled current source (VCCS)is one that supplies a current whose magnitude $I_o = kV_i$ is independent of the load to which the current is supplied.

*k has the dimensions of siemens. it relates output current to input voltage, it is called the transconductance, **gm**, of the source. (Figure 3-10)*

In Fig 3-10(a), v^- is virtual ground, so $I_1 = V_{in}/R_1$. Since no current flows into the inverting terminal of the ideal amplifier, $I_L = I_1$, or

$$I_L = V_{in} / R_1 \text{----------3-23}$$

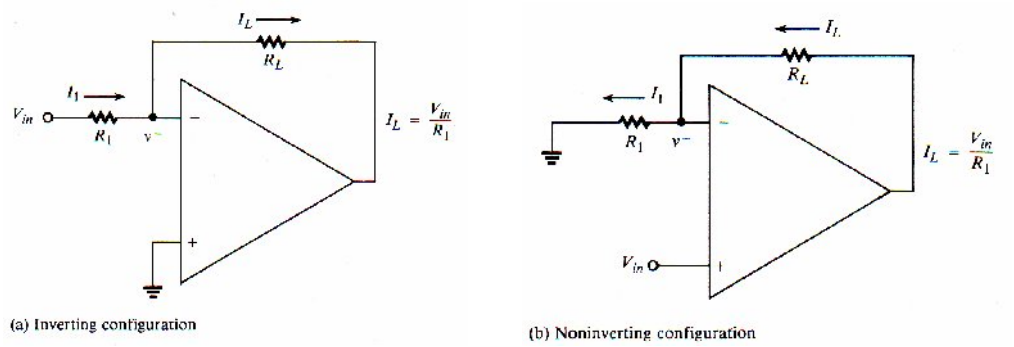


Figure 3-10 Floating-load, voltage-controlled current sources

gm = $1/R_1$ siemens. The load is a floating load, because neither side of R_L can be grounded. In Fig 3-10(b), $v^- = V_{in}$, so $I_1 = V_{in}/R_1$. Once again, no current flows into the inverting terminal, so $I_L = I_1$. Therefore

$$I_L = V_{in}/R_1 \text{----------3-24}$$

gm = $1/R_1$ siemens. The load is also floating in this version.

For successful operation, the load resistance in each circuit must obey

$$R_L < \frac{R_1|V_{max}|}{V_{in}} \quad \text{(inverting circuit)} \text{----------3-25}$$

$$R_L < R_1\left(\frac{|V_{max}|}{V_{in}} - 1\right) \quad \text{(noninverting circuit)} \text{----------3-26}$$

Where $|V_{max}|$ is the magnitude of the maximum output voltage of the amplifier.

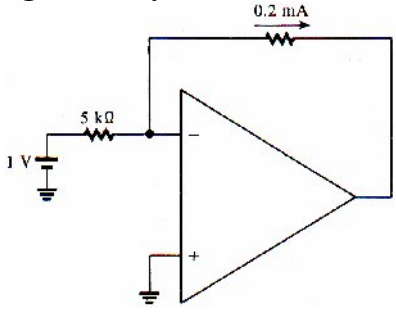


Figure 3-11 (Ex 3-5)

Example 3-5. *Design an inverting, VCCS that will supply a constant current of 0.2mA when the controlling voltage is 1V. What is the maximum load resistance for this supply if the maximum amplifier output voltage is 20V?*

Solution. *gm = (0.2mA)/(1V) = 0.2 X 10^{-3} S. $R_1 = 1/gm = 5$ kΩ.*

$$R_L < \frac{R_1|V_{max}|}{V_{in}} = \frac{(5\text{ k}\Omega)(20\text{ k}\Omega)}{1\text{ V}} = 100\text{ k}\Omega$$

refer to Fig 3-12(b). Since there is (ideally) zero current into the + input, KCL at the node where R_L is connected to the + input gives

$$I_L = I_1 + I_2 \text{----------3-27}$$

$$I_L = \frac{V_{in} - V_L}{R} + \frac{V_o - V_L}{R} \text{----------3-28}$$

By voltage-divider action

$$v^- = \left(\frac{R}{R+R}\right)V_o = V_o/2 \text{----------3-29}$$

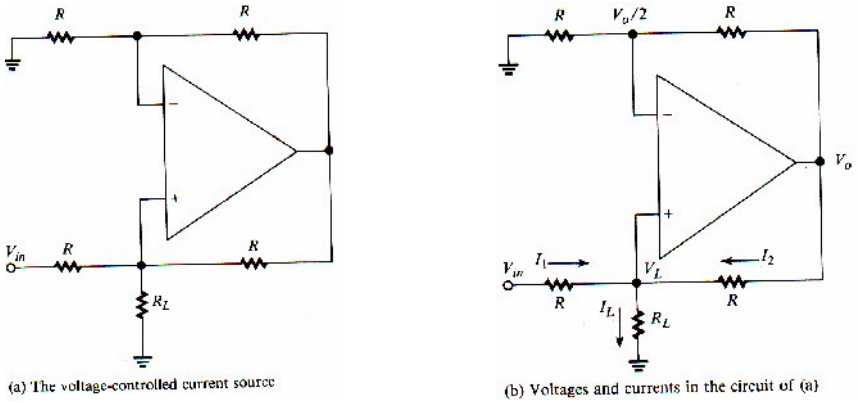


Figure 3-12 A voltage-controlled current source with a grounded load

Since $v^- = v^+ = V_L$, *we have* $V_L = vo/2$, *substitution in (3-28), gives* $I_L = \frac{V_{in}}{R} - \frac{V_o}{2R} + \frac{V_o}{R} - \frac{V_o}{2R}$

$$I_L = V_{in}/R \text{----------3-30}$$

$$R_L < \frac{R|V_{max}|}{2V_{in}} \text{----------3-31}$$

Example 3-6. *Find the current through each resistor and the voltage at each node of the VCCS Fig 3-13. What is the transconductance of the source?*

Solution. $I_L = V_{in}/R = (10V)/(4\ k\Omega) = 2.5mA.$

The voltage at node C (V_L) *is :* $V_c = I_L R_L = (2.5\ mA)(1.5\ k\Omega) = 3.75\ V.$

The voltage at node B is twice V_c ($V_o = 2V_L$): $V_B = 2V_c = 2(3.75) = 7.5\ V.$

The voltage at node A is 1/2 at node B ($v^- = V_o/2$): $V_A = (1/2)(V_B) = (1/2)(7.5) = 3.75\ V.$

The currents I_1, I_2, I_3 & I_4 *in* R_1, R_2, R_3, & R_4 *can then be found:*

$$I_1 = (V_{in} - V_C)/R_1 = (10 - 3.75)/(4 \times 10^3) = 1.5625\ \text{mA}$$
$$I_2 = (V_B - V_C)/R_2 = (7.5 - 3.75)/(4 \times 10^3) = 0.9375\ \text{mA}$$
$$I_3 = V_A/R_3 = 3.75/(4 \times 10^3) = 0.9375\ \text{mA}$$
$$I_4 = (V_B - V_A)/R_4 = (7.5 - 3.75)/(4 \times 10^3) = 0.9375\ \text{mA}$$

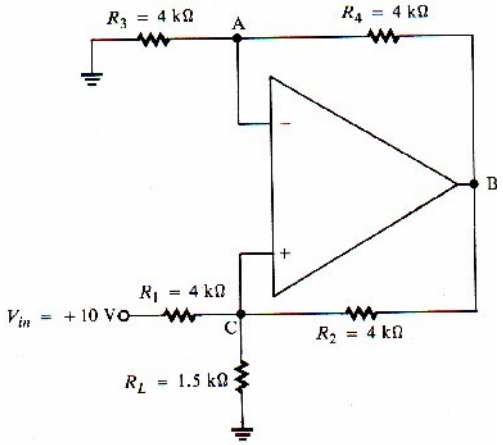


Fig 3-13 Ex 3-6

3-3-3 Current-Controlled Voltage Sources

An ideal current-controlled voltage source (CCVS)has an output voltage $V_o = k\ I_i$ *independent of the load connected to it. k has the units of ohms.CCVS can be thought of as a current-to-voltage converter, since* V_o *is proportional to input current. Since no current flows into the - input, the controlling current* I_{in} *is the same as the current in feedback resistor R. Since* v^- *is virtual ground*

$$V_o = -I_{in}R \text{ ----------3-32}$$

The amplifier has zero output resistance i.e. the output voltage will be independent of load.

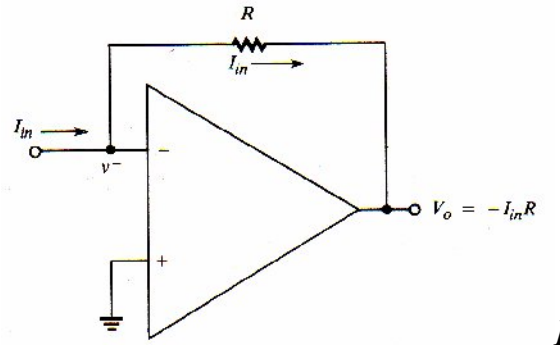


Fig 3-14 A CCVS

3-3-4 Current-Controlled Current Sources

An ideal current-controlled current source (CCCS)is one that supplies a current whose magnitude: I_o=K I_i is independent of the load to which the current is supplied. k is dimensionless.

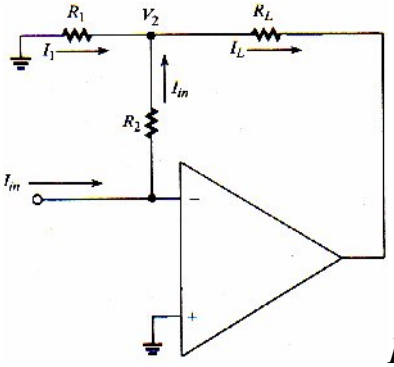


Fig 3-15 CCCS with floating load

Since no current flows into the - input, the current in R_2 must equal I_{in}. Since v^- is at virtual ground, the voltage V_2 is

$$V_2 = -I_{in}R_2 \text{ ----------3-33}$$

Therefore, the current I_1 in R_1 is

$$I_1 = (0 - V_2)/R_1 = I_{in}R_2/R_1 \text{ ----------3-34}$$

Writing KCL at the junction of R_1, R_2, and R_L, we have

$$I_L = I_1 + I_{in} \text{ ----------3-35}$$

Or

$$I_L = \frac{R_2}{R_1} I_{in} + I_{in} = \left(\frac{R_2}{R_1} + 1\right) I_{in} \text{ ----------3-36}$$

For successful operation, R_L must obey

$$R_L < \left(\frac{|V_{max}|}{I_{in}} - R_2\right)\left(\frac{R_1}{R_1 + R_2}\right) \text{ ----------3-37}$$

The amplification factor being

$$k = I_L/I_{in} = 1 + R_2/R_1 \text{ ----------3-38}$$

***Example 3-7**. It is desired to measure a dc current that ranges from 0 to 1 mA using an ammeter whose most sensitive range is 0 to 10 mA. To improve the measurement accuracy, the current to be measured should be amplified by a factor of 10.*

1. Design the circuit.
2. Assuming that the meter resistance is 150 Ω and the maximum V_O of the amplifier is 15 V,
Solution

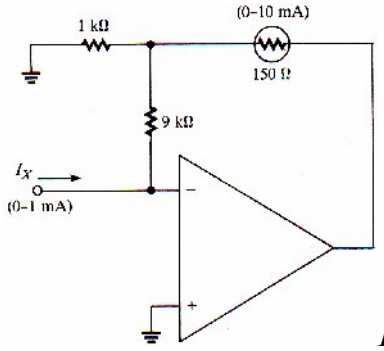


Fig 3-16 Ex 3-7 CCCS as a current amp so a 0-1mA be 0-10 mA

1. I_X is the current to be measured, and the ammeter serves as the load through which the amplified current flows.
The current amplification is $I_L/I_X = 1 + R_2/R_1 = 1 + (9\ k\Omega)/(1\ k\Omega) = 10$
2. when I_{in} = 1 mA:

$$R_L < \left[\frac{15\ \text{V}}{1\ \text{mA}} - (9\ \text{k}\Omega)\right]\left[\frac{1\ \text{k}\Omega}{(1\ \text{k}\Omega) + (9\ \text{k}\Omega)}\right] = 600\ \Omega$$

Since the meter resistance is 150 Ω, the circuit operates satisfactorily.

3-4 Integration, Differentiation,& Waveshaping
3-4-1 Electronic Integration

An electronic integrator is a device that produces an output waveform whose value at any instant of time equals the total area under the input waveform up to that point in time.

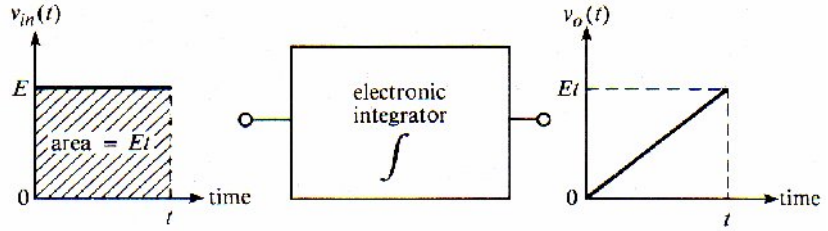


Figure 3-17 The output of the integrator at t seconds is the area, Et, under the input waveform.

the mathematical integration, the process produces the time-varying function $\int_0^t vin(t)dt$.

the input to an electronic integrator is the dc level E volts, which is first connected to the integrator at an instant of time t = 0.

At any time-point t, the total area under the input waveform between time 0 and time t is ***(height) x (width) = Et*** *volts.*

if E = 5 V dc, vo will be 5V at t =1s, 10V at t =2 s, 15V at t =3 s, & so vo(t) = Et.
Fig 3-18 . The component in the feedback path is capacitor C, the amplifier(ideal) is operated in an inverting configuration. we are assuming zero input offset.
to represent integration of the voltage v between time 0 and time t, the output of this circuit is

$$v_O(t) = \frac{-1}{R_1 C}\int_0^t v_{in}\, dt \qquad \text{----------3-39}$$

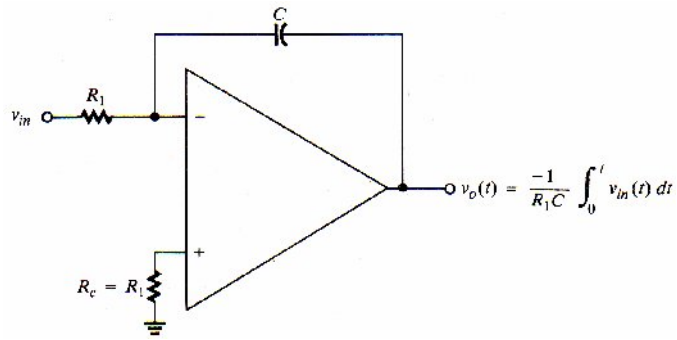


Figure 3-18 An ideal electronic integrator

This equation shows that the output is the (inverted) integral of the input, multiplied by the constant $1/R_1C$. If this circuit were used to integrate the dc waveform shown in Figure3-17, the output would be a negative-going ramp ($vo = -Et/R_1C$).

Since the current into the - input is 0, we have, from Kirchhoff's current law

$$i_1 + i_C = 0 \qquad \text{----------3-40}$$

i_1 is the input current through R_1 and ic is the feedback current through the capacitor. Since $v^- = 0$, the current in the capacitor is

$$i_C = C\frac{dv_o}{dt} \qquad \text{----------3-41}$$

thus

$$\frac{v_{in}}{R_1} + C\frac{dv_o}{dt} = 0 \qquad \text{----------3-42}$$

or

$$\frac{dv_o}{dt} = \frac{-1}{R_1 C}\, v_{in} \qquad \text{----------3-43}$$

Integrating both sides with respect to t, we obtain

$$v_o = \frac{-1}{R_1 C}\int_0^t v_{in}\, dt \qquad \text{----------3-44}$$

It can be shown, using calculus, that the mathematical integral of the sine wave A sin wt is

$$\int (A \sin \omega t)\, dt = \frac{-A}{\omega}\sin(\omega t + 90°) = \frac{-A}{\omega}\cos(\omega t)$$

when the input to the inverting integrator in Figure 3-18 is vin = A sin wt, the output is

$$v_o = \frac{-1}{R_1 C}\int (A \sin \omega t)\, dt = \frac{-A}{\omega R_1 C}(-\cos \omega t)$$

$$= \frac{A}{\omega R_1 C}\cos \omega t \qquad \text{----------3-45}$$

Eq 3-45 the output of an integrator with sinusoidal input is a sinusoidal waveform whose amplitude is inversely proportional to its frequency. This observation follows from the presence of w (= 2πf) in the denominator of (3-45) . if a 100-Hz input sine wave produces an output with peak value 10V, then, all else being equal, a 200-Hz sine wave will produce an output with peak value 5V. Note also that the output leads the input by 90°, regardless of frequency, since cos wt = sin(wt + 90°).

Example 3-8.*1. Find the peak value of the output of the ideal integrator shown in Figure 3-19. The input is vin = 0.5 sin (100t) V.*
2. Repeat, when vin = 0.5 sin (10^3 t) V.

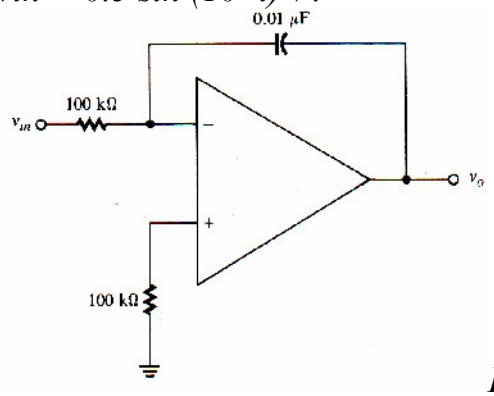


Figure 3-19 (Example 3-8)

Solution.1.

$$v_o = \frac{A}{\omega R_1 C}\cos(\omega t) = \frac{0.5}{100(10^5)(10^{-8})}\cos(100t)$$
$$= 5\cos(100t)\ \text{V} \qquad \text{peak value} = 5\ \text{V}$$

2.

$$v_o = \frac{0.5}{1000(10^5)(10^{-8})}\cos(1000t)$$
$$= 0.5\cos(1000t)\ \text{V} \qquad \text{peak value} = 0.5\ \text{V}$$

Gain magnitude is the ratio of the peak value of the output to the peak value of the input:

$$\left|\frac{v_o}{v_{in}}\right| = \frac{A}{A\omega R_1 C} = \frac{1}{\omega R_1 C} \text{---------3-46}$$

gain is inversely proportional to frequency. Because the integrator's output amplitude decreases with frequency, it is a kind of low-pass filter.

5-1-1 Practical Integrators

any input offset is integrated as if it were a dc signal input and will eventually cause the amplifier to saturate. To eliminate this problem in practical integrators using general-purpose amplifiers, a resistor is connected in parallel with the feedback capacitor.
Since the capacitor is an open circuit as dc is concerned, the dc closed-loop gain of the integrator is $-R_f/R_1$. At high frequencies, Xc is much smaller than Rf. so the parallel combination of C and R_f is essentially the same as C alone, and signals are integrated as usual. we can say that satisfactory integration will occur at frequencies much greater than the frequency at which Xc = R_f. That is, for integrator action we want

$$X_C << R_f \quad \ldots\ldots\ldots \quad \frac{1}{2\pi f C} << R_f$$

$$f >> \frac{1}{2\pi R_f C} \text{----------3-47}$$

The frequency f_c where Xc= R_f

$$f_c = \frac{1}{2\pi R_f C} \text{----------3-47a}$$

at frequencies well above f_c. the gain falls off at the rate of -20 dB/decade, like that of an ideal integrator, and at frequencies below f_c. the gain approaches its dc value of R_f/R_1.

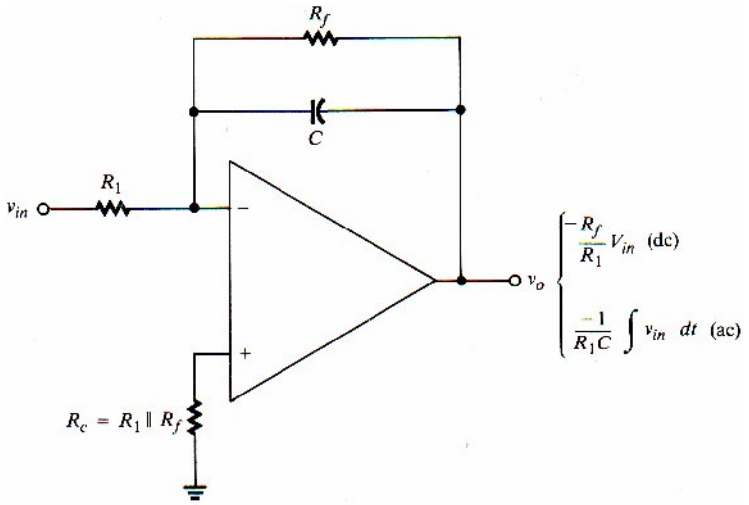


Figure 3-20 A resistor Rf connected in parallel with C causes the practical integrator to behave like an inverting amplifier to dc inputs and like an integrator to high-frequency ac inputs.

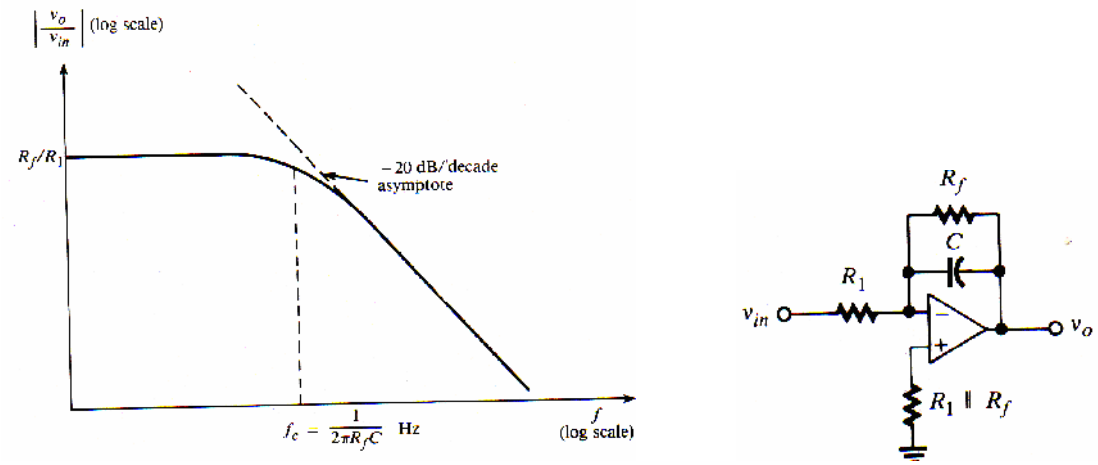


Figure 3-21 Bode plot for a practical integrator, showing that integration occurs at frequencies above $1/(2\pi R_f C)$ Hz

***Example 3-9**. Design a practical integrator that*
1. integrates signals with frequencies down to 100 Hz.
2. produces a peak output of 0.1V when vin is a 10V-peak sine wave at frequency 10 kHz.
Find the dc component in the output when there is a + 50mV dc input.
***Solution**.*
1. we require fc << 100Hz. choose fc one decade below 100Hz: fc = 10 Hz. Then

$$f_c = 10 = \frac{1}{2\pi R_f C}$$

Choose C = 0.01μF. Then

$$10 = \frac{1}{2\pi R_f (10^{-8})}$$

$$R_f = \frac{1}{2\pi(10)(10^{-8})} = 1.59\ \text{M}\Omega$$

2. we must choose R_1 so that the gain at 10 kHz is

$$\left|\frac{v_o}{v_{in}}\right| = \frac{0.1\ \text{V}}{10\ \text{V}} = 0.01$$

Assuming that we can neglect R_f at this frequency (3 decades above fc), the gain is the same as that for an ideal integrator:

$$\left|\frac{v_o}{v_{in}}\right| = \frac{1}{\omega R_1 C} = 0.01$$

$$\frac{1}{2\pi \times 10^4 R_1(10^{-8})} = 0.01$$

$$R_1 = \frac{1}{2\pi \times 10^4 \times (0.01 \times 10^{-8})} = 159\ \text{k}\Omega$$

The required circuit is shown in Figure 3-22. Note that Rc =(1.59 MΩ)‖(159kΩ)=145kΩ.

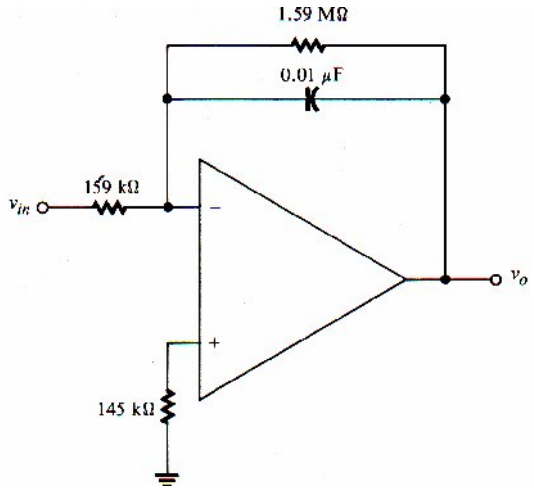


Figure 3-22 (Example 3-9)

When the input is 50 mV dc, the output is 50 mV times the dc closed-loop gain:

$$v_o = \frac{-R_f}{R_1}(50\ \text{mV}) = \frac{-1.59\ \text{M}\Omega}{159\ \text{k}\Omega}(50\ \text{mV}) = -0.5\ \text{V}$$

5-2 Electronic Differentiation

An electronic differentiator produces an output waveform whose value at any instant of time is equal to the rate of change of the input at that point in time.

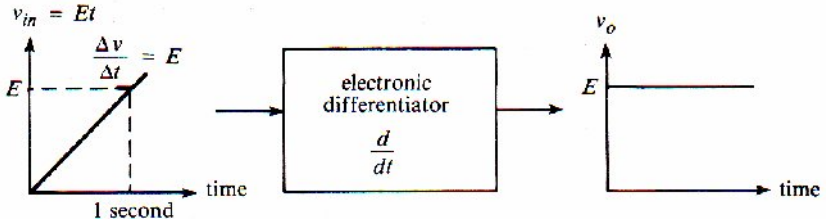


Figure 3-23 The ideal electronic differentiator produces an output equal to the rate of change of the input. Since the rate of change of a ramp is constant, the output in this example is a dc level.

Fig 3-23 an ideal electronic differentiator, vin = Et. The rate of change, of this ramp is a constant E volts/second. Since the rate of change of the input is constant, the output of the differentiator is the constant dc level E volts. we would write

$$\frac{dv_{in}}{dt} = \frac{d(Et)}{dt} = E$$

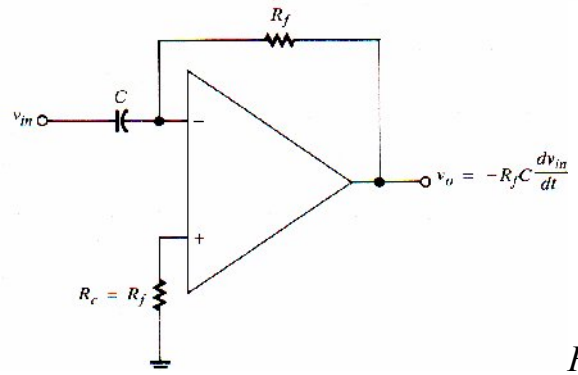


Figure 3-24 An ideal electronic differentiator

now have a capacitive input and a resistive feedback-again, just the opposite of an integrator. It can be shown that the output of this differentiator is
Since the current into the - terminal is 0, we have, from KCL,

$$i_C + i_f = 0 \text{----------3-48}$$

Since v⁻ = 0, vc = vin and

$$i_C = C\frac{dv_{in}}{dt} \text{---------3-49}$$

Also, if = vo /Rf , so

$$C\frac{dv_{in}}{dt} + \frac{v_o}{R_f} = 0$$

$$v_o = -R_f C \frac{dv_{in}}{dt} \text{----------3-50}$$

$$\frac{d(A \sin \omega t)}{dt} = A\omega \cos \omega t \text{----------3-51}$$

When the input is vin = A sin wt, the output is

$$v_o = -R_f C \frac{d(A \sin \omega t)}{dt} = -A\omega R_f C \cos(\omega t) = A\omega R_f C \sin(\omega t - 90°) \text{---------3-52}$$

when the input is sinusoidal, the amplitude of the output of a differentiator is directly proportional to frequency .also the output lags the input by 90°, regardless of frequency. The gain of the differentiator is

$$\left|\frac{v_o}{v_{in}}\right| = \frac{A\omega R_f C}{A} = \omega R_f C \text{----------3-53}$$

5-2-1 Practical Differentiators

In a practical differentiator, the amplification of signals in direct proportion to their frequencies cannot continue as frequency increases, because the amplifier has a finite bandwidth, there is some frequency at which the output amplitude must begin to fall off, so that it will have a break frequency even lower than that determined by the upper cutoff frequency . This action is accomplished by connecting a resistor in series with the input capacitor, as shown in Fig 3-25.

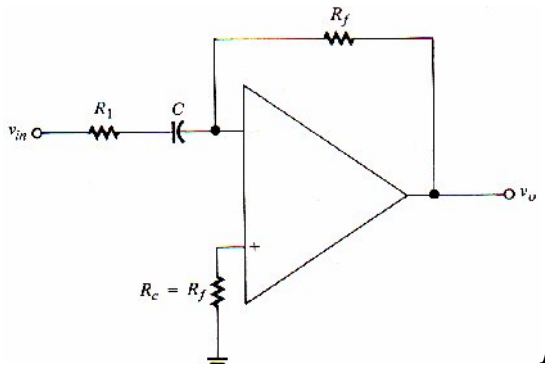


Fig 3-25 A practical differentiator. Differentiation occurs at low frequencies, but resistor R_1 prevents high-frequency differentiation.

The net impedance of the R_1C combination at low and high frequencies:

$$Z_{in} = R_1 - j/\omega C \quad \text{----------3-54}$$

$$|Z_{in}| = \sqrt{R_1^2 + (1/\omega C)^2} \quad \text{----------3-55}$$

The break frequency f_b is the frequency at which the Xc = R_1:

$$\frac{1}{2\pi f_b C} = R_1 \quad \text{----------3-56}$$

$$f_b = \frac{1}{2\pi R_1 C} \text{ Hz}$$

the break frequency should be set well above the highest frequency at which accurate differentiation is desired:

$$f_b >> f_h \quad \text{----------3-57}$$

where f_h is the highest differentiation frequency

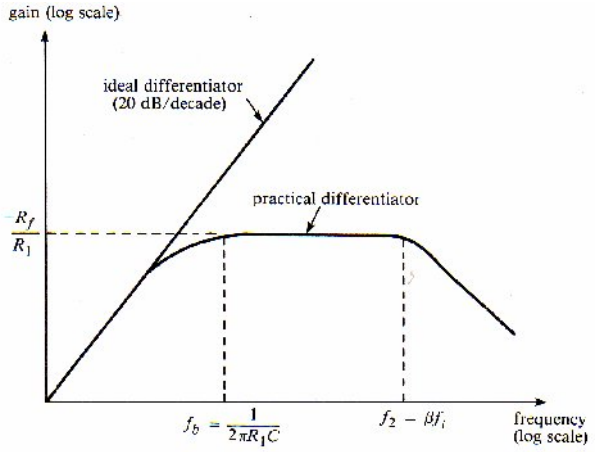


Figure 3-26 Bode plots for the ideal and practical differentiators. f_b is the break frequency due to the input R_1C combination and f_2 is the upper cutoff frequency of the (dosed-loop) amplifier.

Fig 3-26 show that the gain rises with frequency at the rate of 20 dB/decade, and the gain levels off beyond the break frequency f_b and then falls off at -20 dB/decade beyond the amplifier's upper cutoff frequency. the closed-loop bandwidth, or upper cutoff frequency is

$$f_2 = \beta f_t \text{----------3-58}$$

where β in this case is $R_1/(R_1 + R_f)$.

Example 3-10.*1. Design a practical differentiator that will differentiate signals with frequencies up to 200 Hz. The gain at 10Hz should be 0.1.*
2. If the operational amplifier used in the design has a unity-gain frequency of 1 MHz. what is the upper cutoff frequency of the differentiator?

Solution.

1. We must select R_1 and C to produce a break frequency f_b that is well above f_h=200Hz. Let us choose $f_b = 10f_h = 2$ kHz. Letting C = 0.1μF,

$$f_b = 2 \times 10^3 = \frac{1}{2\pi R_1 C}$$

$$R_1 = \frac{1}{2\pi(2 \times 10^3)(10^{-7})} = 796\ \Omega$$

In order to achieve a gain of 0.1 at 10 Hz,

$$\left|\frac{v_o}{v_{in}}\right| = 0.1 = \omega R_f C = (2\pi \times 10)R_f(10^{-7})$$

$$R_f = \frac{0.1}{2\pi \times 10 \times 10^{-7}} = 15.9\ \text{k}\Omega$$

The completed design in shown in Figure 3-27.

2.

$$\beta = \frac{R_1}{R_1 + R_f} = \frac{796}{796 + 15.9 \times 10^3} = 0.0477$$

$f_2 = \beta f_t$ = (0.0477)(1 MHz) = 47.7 kHz. The Bode plot is sketched in Figure 3-28

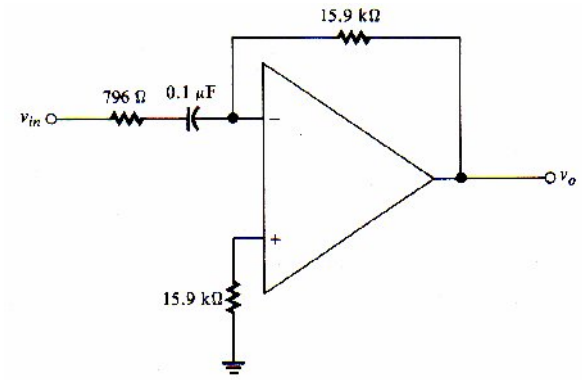


Figure 3-27 (Example 3-10)

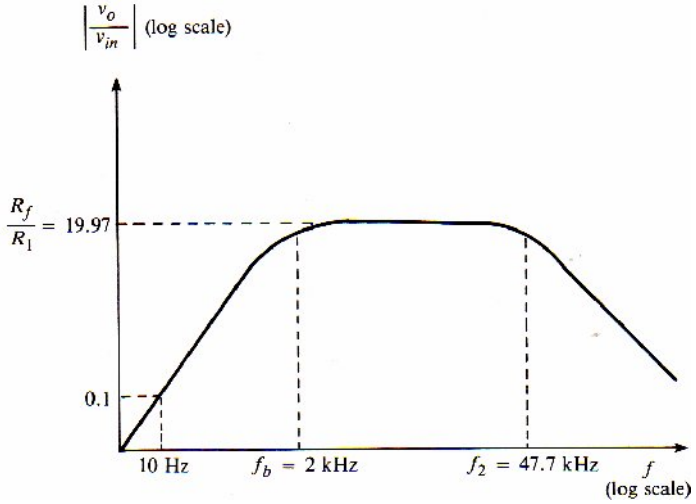


Figure 3-28 (Example 3-10)

6- Instrumentation Amplifiers

an amplifier can be operated in a differential mode to produce an output voltage proportional to the difference between two input signals . Figure 3-29 shows an improved configuration for producing an output proportional to the difference between two inputs. This circuit arrangement is so commonly used that it is called an instrumentation amplifier.

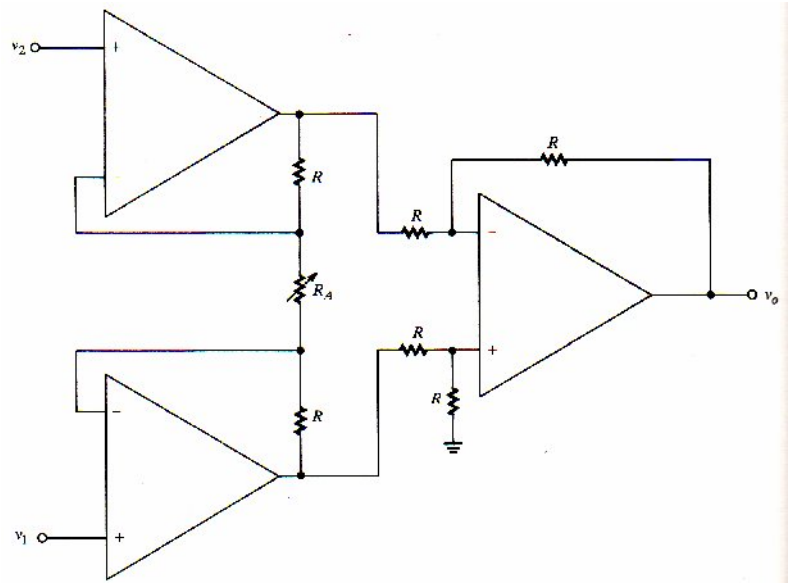


Figure 3-29 An instrumentation amplifier that produces an output proportional to v_1 - v_2. Adjustable resistor R_A is used to set the gain

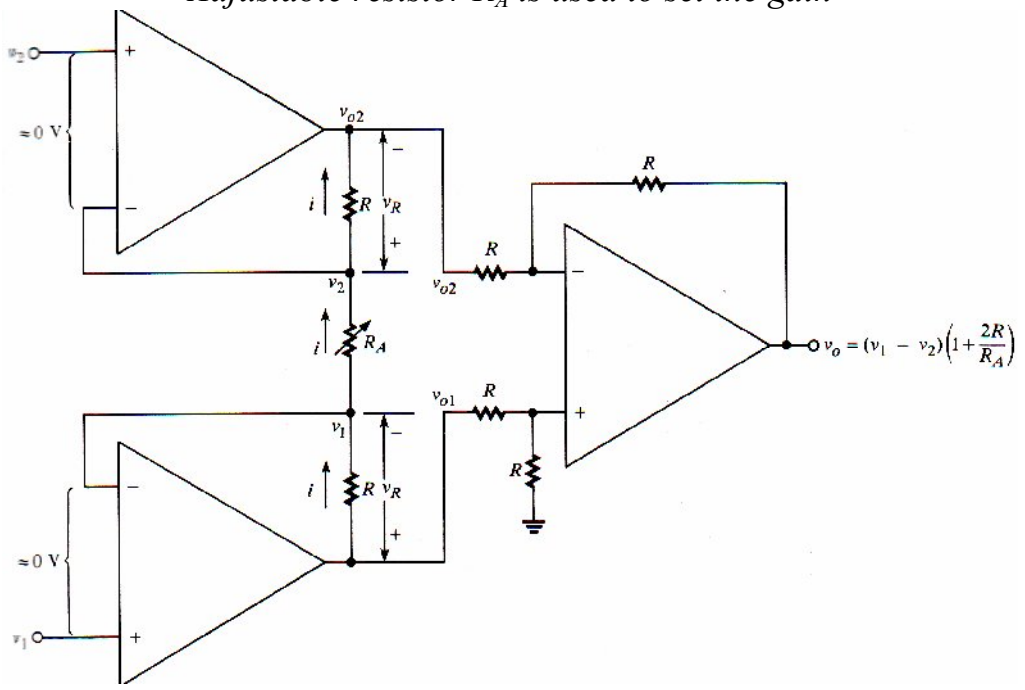


Figure 3-30 Voltage and current relations in the instrumentation amplifier. Note that the overall gain is inversely proportional to the value of adjustable resistor R_A.

Figure 3-30. For analysis, let us assume that $v_1 > v_2$. Then, the current i through R_A is

$$i = \frac{v_1 - v_2}{R_A} \qquad \text{----------3-59}$$

Since no current flows into either amplifier input terminal, the current i must also flow in each resistor R connected on opposite sides of R_A. Therefore, the voltage drop across each of those resistors is

$$v_R = iR = \frac{(v_1 - v_2)R}{R_A} \qquad \text{----------3-60}$$

The output voltages vo_1 and vo_2 are given by

$$v_{o1} = v_1 + v_R \text{ ----------3-61}$$

And

$$v_{o2} = v_2 - v_R \text{ ----------3-62}$$

Voltages vo_1 and vo_2 are the input voltages to the differential stage . Since the external resistors connected to that stage are all equal to R,

$$v_o = v_{o1} - v_{o2} \text{ ----------3-63}$$

$$v_o = (v_1 + v_R) - (v_2 - v_R) = v_1 - v_2 + 2v_R \text{ ----------3-64}$$

$$v_o = v_1 - v_2 + \frac{2(v_1 - v_2)R}{R_A} = (v_1 - v_2)(1 + 2R/R_A) \text{ ----------3-65}$$

Vo proportional to $(v_1 - v_2)$. The overall closed-loop gain = $(1 + 2R/R_A)$. R_A is made adjustable so that gain can be easily adjusted for calibration purposes.
To ensure proper operation of the instrumentation amplifier, all three of the following inequalities must be satisfied at all times:

$$\left| \left(1 + \frac{R}{R_A}\right) v_1 - \frac{R}{R_A} v_2 \right| < |V_{\max(1)}| \text{ ----------3-66}$$

$$\left| \left(1 + \frac{R}{R_A}\right) v_2 - \frac{R}{R_A} v_1 \right| < |V_{max(1)}| \text{ ----------3-67}$$

$$\left(1 + \frac{2R}{R_A}\right) |v_1 - v_2| < |V_{max(2)}| \text{ ----------3-68}$$

$V_{max(1)}$ is the maximum output voltage of each input stage
$V_{max(2)}$ is the maximum output voltage of the differential stage.

Example 3-11.*1. Assuming ideal amplifiers, find $V_{o(min)}$ and $V_{o(max)}$ of the instrumentation amplifier shown in Fig 3-31 when the 10-kΩ potentiometer Rp is adjusted through its entire range.*
2. Find $\boldsymbol{V_{o1}}$ and $\boldsymbol{V_{o2}}$ when Rp is set in the middle of its resistance range.
Solution.
1. R_A = Rp +500Ω resistor. Assuming that Rp can be adjusted through a full range from 0 to 10 kΩ.

$$R_{A(min)} = 500\ \Omega$$

$$R_{A(max)} = (500\ \Omega) + (10\ k\Omega) = 10.5\ k\Omega.$$

$$v_o(\min) = (V_1 - V_2)\left[1 + \frac{2R}{R_A(\max)}\right] = [0.3 - (-0.2)] \times \left[1 + \frac{2(10\ k\Omega)}{10.5\ k\Omega}\right]$$

$$= 1.45\ V$$

$$v_o(\max) = (V_1 - V_2)\left[1 + \frac{2R}{R_A(\min)}\right] = [0.3 - (-0.2)] \times \left[1 + \frac{2(10\ k\Omega)}{500\ \Omega}\right]$$

$$= 20.5\ V$$

2. When $R_A = 500 + (1/2)(10 \times 10^3) = 5.5\ k\Omega$,

$$V_R = \frac{(V_1 - V_2)R}{R_A} = \frac{[0.3 - (-0.2)]\ 10 \times 10^3}{5.5 \times 10^3} = 0.909\ \text{V}$$

$$V_{o1} = V_1 + V_R = 0.3 + 0.909 = 1.209\ \text{V}$$

$$V_{o2} = V_2 - V_R = -0.2 - 0.909 = -1.109\ \text{V}$$

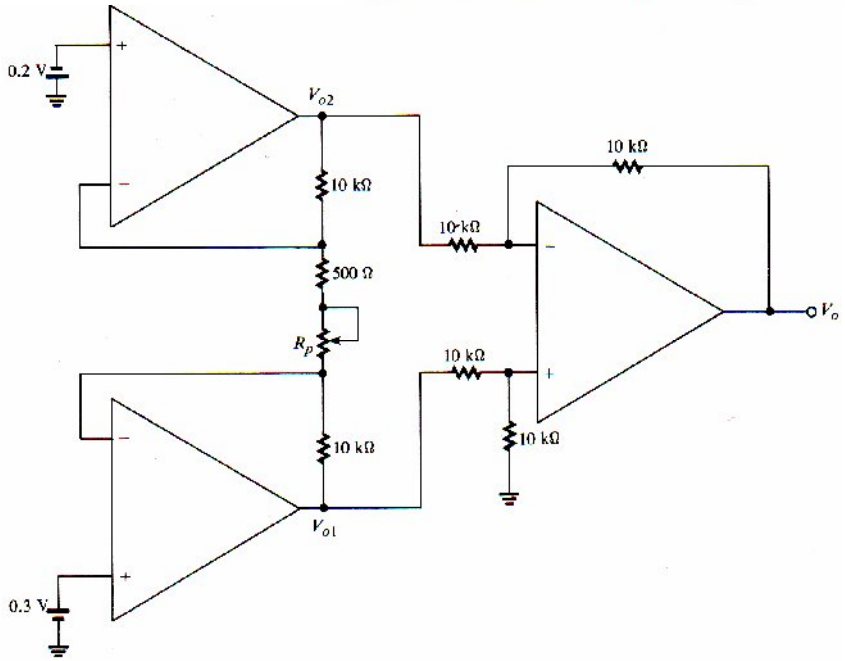


Figure 3-31 Example3-11

Example 3-12. *The maximum output voltages for all three operational amplifiers in an instrumentation amplifier are ± 15 V. For a particular application, it is known that input signal v_1 may vary from 0 V to 0.8 V and input signal v_2 from 0 V to 1.3 V. Assuming that R = 2 kΩ, design the circuit for maximum possible closed-loop gain.*

Solution.

Since the closed-loop gain is inversely proportional to R_A , we must find the minimum value of R_A . We must consider the worst-case condition for each inequality, that is, the combination of values for v_1 and v_2 that makes the left side of each inequality as large as possible. Thus we must satisfy both of the following:

$$\left|\left(1 + \frac{R}{R_A}\right)v_1(\text{max}) - \left(\frac{R}{R_A}\right)v_2(\text{min})\right| < |V_{max}|$$

$$\left|\left(1 + \frac{2 \times 10^3}{R_A}\right)(0.8) - \left(\frac{2 \times 10^3}{R_A}\right)0\right| < 15$$

$$(0.8)\left(\frac{2 \times 10^3}{R_A}\right) < 14.2$$

$$R_A > 112.68\Omega$$

$$\left|\left(1 + \frac{R}{R_A}\right)v_1(\text{min}) - \left(\frac{R}{R_A}\right)v_2(\text{max})\right| < |V_{max}|$$

$$\left|\left(1 + \frac{2 \times 10^3}{R_A}\right)0 - \left(\frac{2 \times 10^3}{R_A}\right)(1.3)\right| < 15$$

$$\frac{2 \times 10^3}{R_A} < 11.54$$

$$R_A > 173.3\Omega$$

$$\left|\left(1+\frac{R}{R_A}\right)v_2-\frac{R}{R_A}v_1\right|<|V_{max(1)}|$$

$$\left|\left(1+\frac{2\times10^3}{R_A}\right)(1.3)-\left(\frac{2\times10^3}{R_A}\right)0\right|<15$$

$$R_A > 189.71\Omega$$

$$\left|\left(1+\frac{2\times10^3}{R_A}\right)(0)-\left(\frac{2\times10^3}{R_A}\right)(0.8)\right|<15$$

$$R_A > 106.67\ \Omega$$

$$\left(1+\frac{2R}{R_A}\right)|v_1-v_2| \quad <|V_{max(2)}|$$

$$\left|\left(1+\frac{4\times10^3}{R_A}\right)(0-1.3)\right|<15$$

$$R_A > 379.56\Omega.$$

$$\left(1+\frac{4\times10^3}{R_A}\right)(0.8-0)\left|<15\right.$$

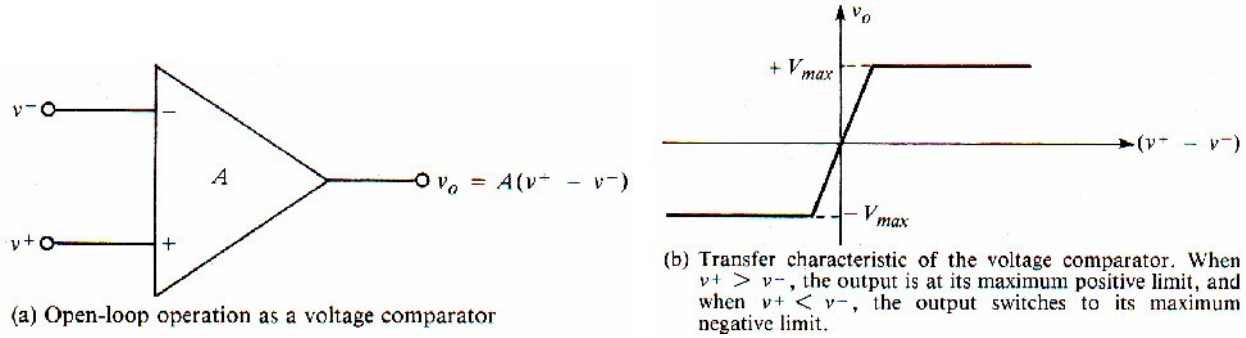
$$R_A > 225.35\ \Omega.$$

Summarizing, we require that all of the following inequalities be satisfied:
$R_A>112.68\Omega$, $R_A>173.3\ \Omega$, $R_A>189.71\ \Omega$, $R_A>106.67\ \Omega$, $R_A>379.56\Omega$, & $R_A>225.35\ \Omega$.
the only way that all inequalities can be satisfied is for R_A to be larger than the largest of the computed limits: $R_A > 379.56\ \Omega$. Choosing the closes: standard 5% resistor value that is larger than 379.56 Ω, we let $R_A = 390\ \Omega$. This choice gives us the maximum permissible closed-loop gain:

$$\frac{v_o}{v_1-v_2}=1+\frac{2R}{R_A}=1+\frac{2(2\times10^3)}{390}=11.26$$

8- Voltage Comparators

It is a device used to compare two voltage levels, the output of the comparator reveals which of its two inputs is larger, so it is a switching device, producing a high output when one input is the larger and a low output if the other input becomes larger. An operational amplifier is used as a voltage comparator by operating it open-loop (no feedback) and by connecting the two voltages to be compared to the inverting and noninverting inputs. if the + input voltage is slightly greater than the - input voltage, the amplifier quickly switches to its maximum positive output, and when the - input voltage is slightly greater than the+ input voltage, the amplifier switches to its maximum negative output.



(a) Open-loop operation as a voltage comparator

(b) Transfer characteristic of the voltage comparator. When $v+ > v-$, the output is at its maximum positive limit, and when $v+ < v-$, the output switches to its maximum negative limit.

Figure 3-32 The operational amplifier used as a voltage comparator

In Fig 3-33 the noninverting input is a 10V-peak sine wave & a +6V-dc source is connected to the inverting input. The comparator output is assumed to switch between ± 15V. Notice that the output switches to +15V each time the sine wave rises through +6V, because $v^+ - v^-$ =(6V) - (6V) = 0V at those points in time. The output remains high so long as $v^+ - v^- > 0$, i.e., v+>6V, and when v+ falls below 6V. the comparator output switches to -15V.

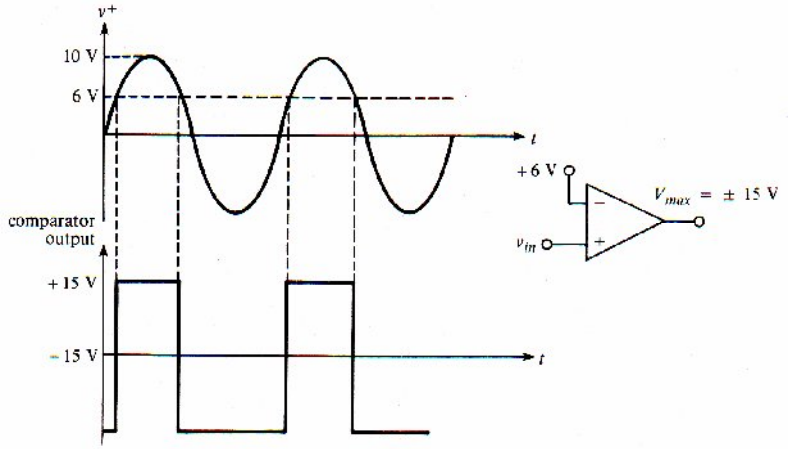


Figure 3-33 The comparator output switches to $+V_{max}$ when $v^+ - v^- > 0$ V, which corresponds to the time points where v^+ rises through +6 V. The output remains high so long as $v^+ - v^- > 0$, or $v^+ > 6$ V.

In some applications, either the inverting or noninverting input is grounded, so the comparator is effectively a zero-crossing detector. It switches output states when the ungrounded input passes through 0. For example, if the inverting input is grounded, the output switches to its maximum positive voltage when v+ is slightly positive and to its maximum negative voltage when v+ is slightly negative. The reverse action occurs if the non inverting input is grounded. shown in Figure 3-34.

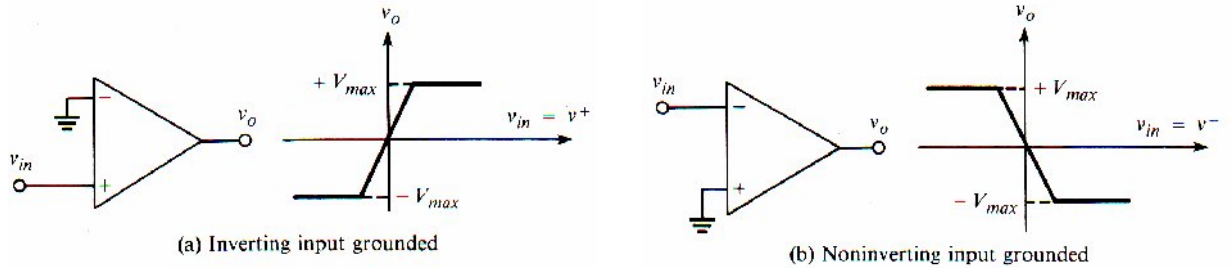


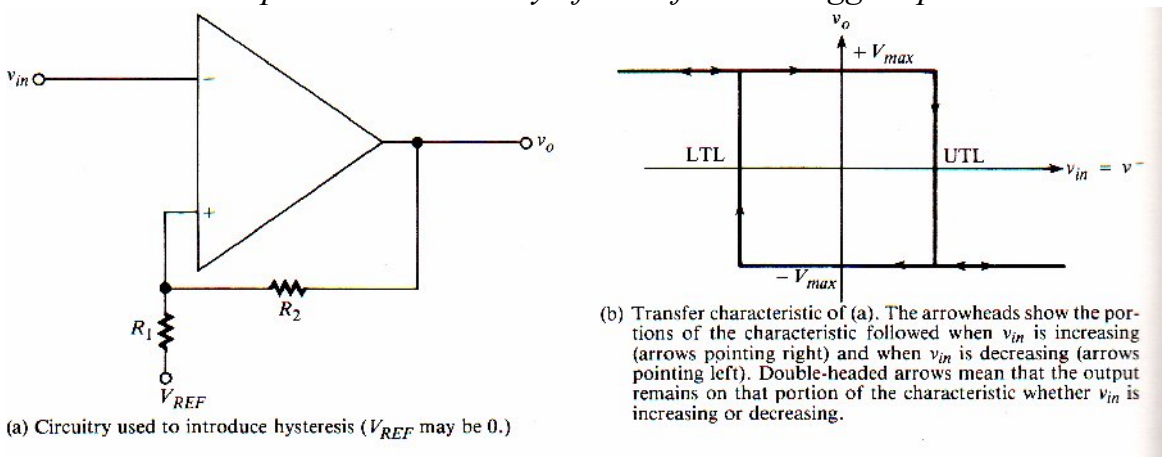
Figure 3-34 Operation of the voltage comparator as a zero-level detector

8- Hysteresis and Schmitt Triggers

hysteresis is a property that means a device behaves differently when its input is increasing from the way it behaves when its input is decreasing. In the context of a voltage comparator, hysteresis means that the output will switch when the input increases to one level but will not switch back until the input falls below a different level. In some applications, hysteresis is a desirable characteristic because it prevents the comparator from switching back .

For example, if $v^+ - v^-$ is near 0 V, and if the input offset voltage is 1 mV, then noise voltages on the order of 1 mV will cause random switching of the comparator output. if the output will switch to one state only when the input rises past -1V, and will switch to the other state only

when the input falls below +1V, then only a very large (2V) noise voltage will cause it to switch states when the input is in the vicinity of one of these "trigger" points.



(a) Circuitry used to introduce hysteresis (V_{REF} may be 0.)

(b) Transfer characteristic of (a). The arrowheads show the portions of the characteristic followed when v_{in} is increasing (arrows pointing right) and when v_{in} is decreasing (arrows pointing left). Double-headed arrows mean that the output remains on that portion of the characteristic whether v_{in} is increasing or decreasing.

Figure 3-35 A voltage comparator with hysteresis (Schmitt trigger)

Fig 3-35, the input is connected to the inverting terminal and a voltage divider is connected across the noninverting terminal between vo and a fixed reference voltage V_{REF} (which may be 0). Fig 3-35(b)(hysteresis loop). This characteristic shows that the output switches to +V max when Vin falls below a lower trigger level (LTL), but will not switch to $-V_{max}$ unless Vin rises past an upper trigger level (UTL). A comparator having this characteristic is called a Schmitt trigger. We can derive expressions for UTL and LTL using the superposition principle. Suppose first that the comparator output is shorted to ground. Then

$$v^+ = \frac{R_2}{R_1 + R_2} V_{REF} \quad (v_o = 0) \qquad \text{----------3-69}$$

When V_{REF} is 0, we find

$$v^+ = \frac{R_1}{R_1 + R_2} v_o \quad (V_{REF} = 0) \qquad \text{----------3-70}$$

Therefore, when the output is at its negative limit (vo = -Vmax),

$$v^+ = \frac{R_2}{R_1 + R_2} V_{REF} + \frac{R_1}{R_1 + R_2} (-V_{max}) \qquad \text{----------3-71}$$

In Figure 3-35(b), v^- must fall to this value of v^+ before the comparator switches to +Vmax Therefore,

$$\text{LTL} = \frac{R_2}{R_1 + R_2} V_{REF} + \frac{R_1}{R_1 + R_2} (-V_{max}) \qquad \text{----------3-72}$$

Similarly, when vo = + Vmax, Vin must rise to

$$\text{UTL} = \frac{R_2}{R_1 + R_2} V_{REF} + \frac{R_1}{R_1 + R_2} (+V_{max}) \qquad \text{----------3-73}$$

+Vmax is the maximum positive output voltage (a positive number) and -Vmax is the maximum negative output voltage (a negative number). The magnitudes of these quantities may be different; the hysteresis of a Schmitt trigger is defined to be the difference between the input trigger levels.

$$\text{Hysteresis} = \text{UTL} - \text{LTL} = \left(\frac{R_1}{R_1 + R_2}\right)(+V_{max}) - \left(\frac{R_1}{R_1 + R_2}\right)(-V_{max}) \qquad \text{----------3-74}$$

If the magnitudes of the maximum output voltages are equal, we have

$$\text{Hysteresis} = \frac{2R_1 V_{max}}{R_1 + R_2} \quad \text{----------3-75}$$

Example 3-13.*1. Find the upper and lower trigger levels and the hysteresis of the Schmitt trigger shown in Fig 3-36. Sketch the hysteresis loop. The output switches between ± 15 V.*
2. Repeat (1) if $V_{REF} = 0$ V.
3. Repeat (1) if $V_{REF} = 0$ V and the output switches between 0 V and + 15V.

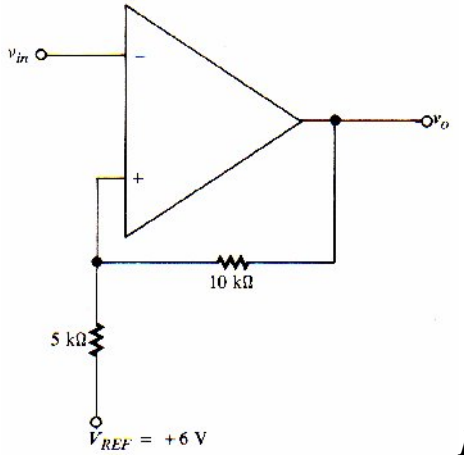


Figure 3-36 (Example 3-13)

Solution.*1.*

$$\text{LTL} = \left[\frac{10\ \text{k}\Omega}{(5\ \text{k}\Omega) + (10\ \text{k}\Omega)}\right](6\ \text{V}) + \left[\frac{5\ \text{k}\Omega}{(5\ \text{k}\Omega) + (10\ \text{k}\Omega)}\right](-15\ \text{V}) = -1\ \text{V}$$

$$\text{UTL} = \left[\frac{10\ \text{k}\Omega}{(5\ \text{k}\Omega) + (10\ \text{k}\Omega)}\right](6\ \text{V}) + \left[\frac{5\ \text{k}\Omega}{(5\ \text{k}\Omega) + (10\ \text{k}\Omega)}\right](15\ \text{V}) = +9\ \text{V}$$

$$\text{Hysteresis} = (9\ \text{V}) - (-1\ \text{V}) = 10\ \text{V}$$

also, hysteresis = 2(5 kΩ)(15 V)/(15 kΩ) = 10 V
2. Since $V_{REF} = 0$

$$\text{LTL} = \left(\frac{R_1}{R_1 + R_2}\right)(-V_{max}) = \left[\frac{5\ \text{k}\Omega}{(5\ \text{k}\Omega) + (10\ \text{k}\Omega)}\right](-15\ \text{V}) = -5\ \text{V}$$

$$\text{UTL} = \left(\frac{R_1}{R_1 + R_2}\right)(+V_{max}) = \left[\frac{5\ \text{k}\Omega}{(5\ \text{k}\Omega) + (10\ \text{k}\Omega)}\right](15\ \text{V}) = +5\ \text{V}$$

$$\text{Hysteresis} = (5\ \text{V}) - (-5\ \text{V}) = 10\ \text{V}$$

3. Since the output switches between 0V &+5V, we must use 0 in place of - Vmax in the trigger-level equations

$$\text{LTL} = \left(\frac{R_1}{R_1 + R_2}\right)(-V_{max}) = \left[\frac{5\ \text{k}\Omega}{(5\ \text{k}\Omega) + (10\ \text{k}\Omega)}\right]0 = 0\ \text{V}$$

$$\text{UTL} = \left(\frac{R_1}{R_1 + R_2}\right)(+V_{max}) = +5\ \text{V}$$

$$\text{Hysteresis} = (5\ \text{V}) - (0\ \text{V}) = 5\ \text{V}$$

Fig 3-37 shows the hysteresis loops for these cases, along with the output wave forms that result when Vin is a 10-V-peak sine wave. The comparator we have discussed is called an inverting Schmitt trigger because the output is high when the input is low, and vice versa.

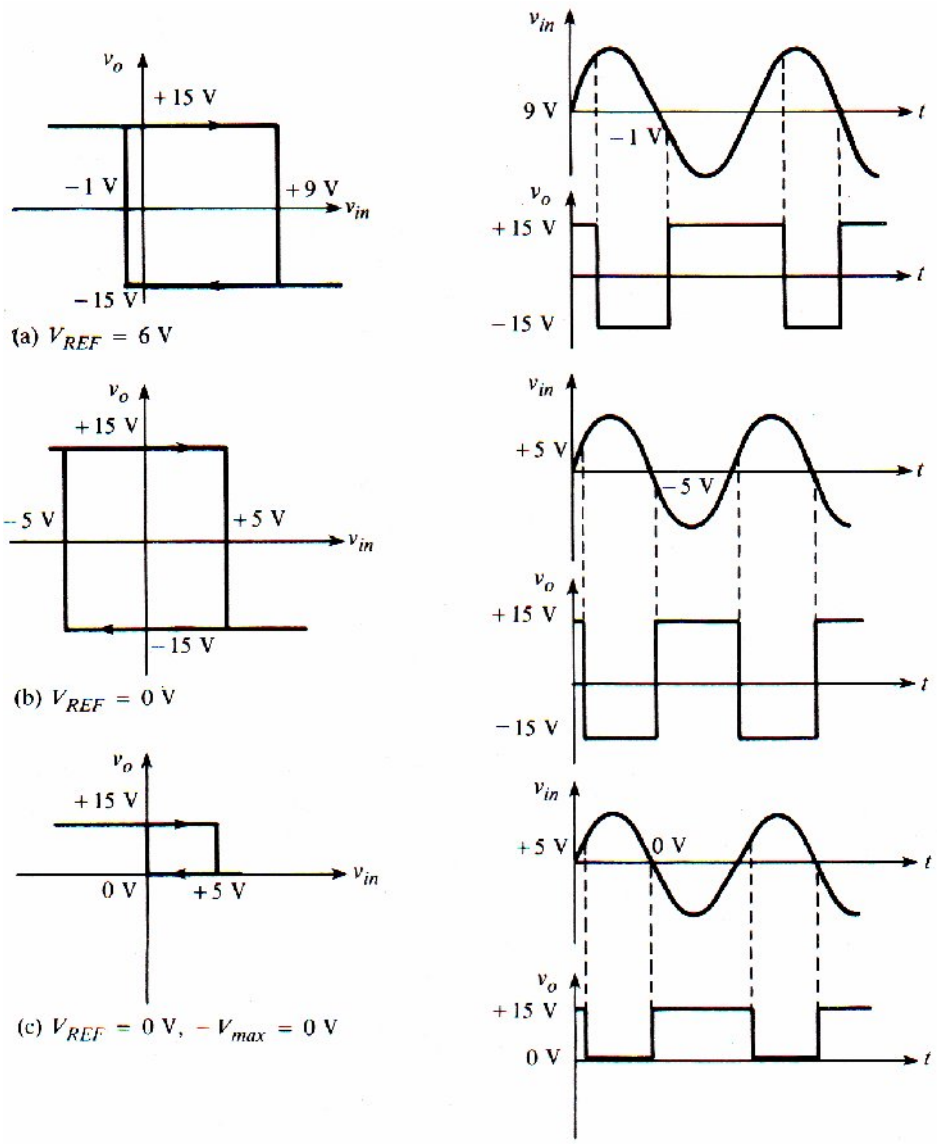


Figure 3-37 Ex 3-13

Figure3-38 shows a noninverting Schmitt trigger , the lower and upper trigger levels are

$$\text{LTL} = \frac{-R_1}{R_2}(+V_{max}) \quad \text{----------3-76}$$

$$\text{UTL} = \frac{R_1}{R_2}\left|-V_{max}\right| \quad \text{----------3-77}$$

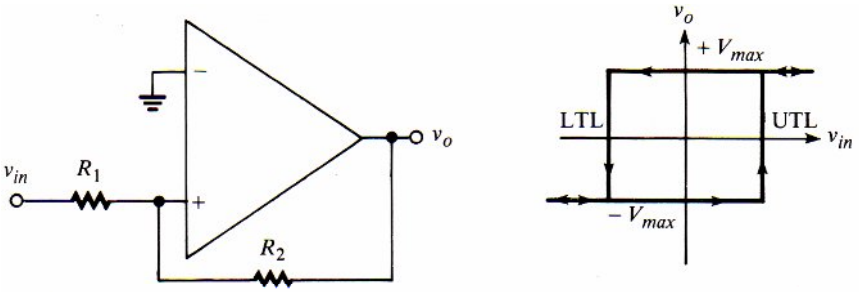


Figure 3-38 The non inverting Schmitt trigger

these equations permit the magnitudes of +Vmax & -Vmax to be different values. For example, if R1 = 10 kΩ & R2 = 20 kΩ, and if the output switches between +10V and -5 V, then LTL = -(0.5)(10 V) = -5V and UTL = 0.5 | -5 V | = +2.5 V.

6- Wave shaping

Wave shaping is the process of altering the shape of a waveform in some prescribed manner to produce a new waveform having a desired shape having precisely the same frequency.

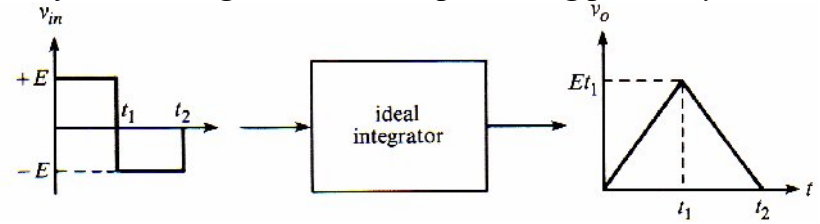
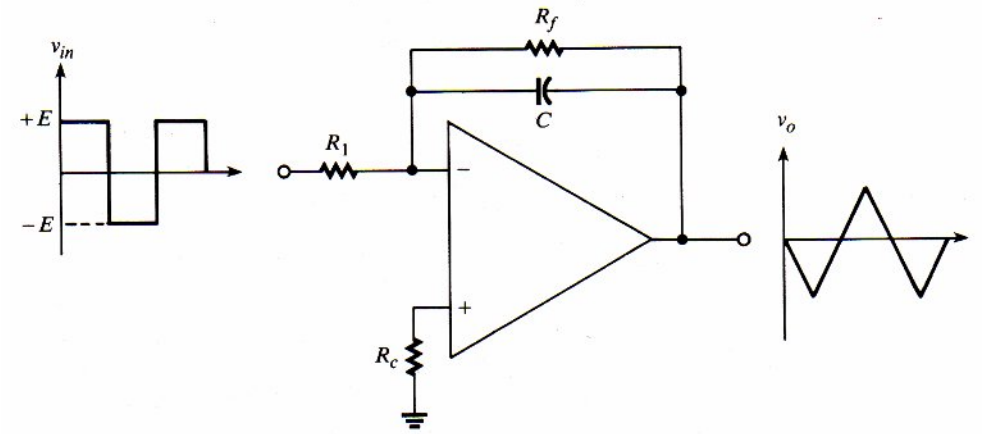
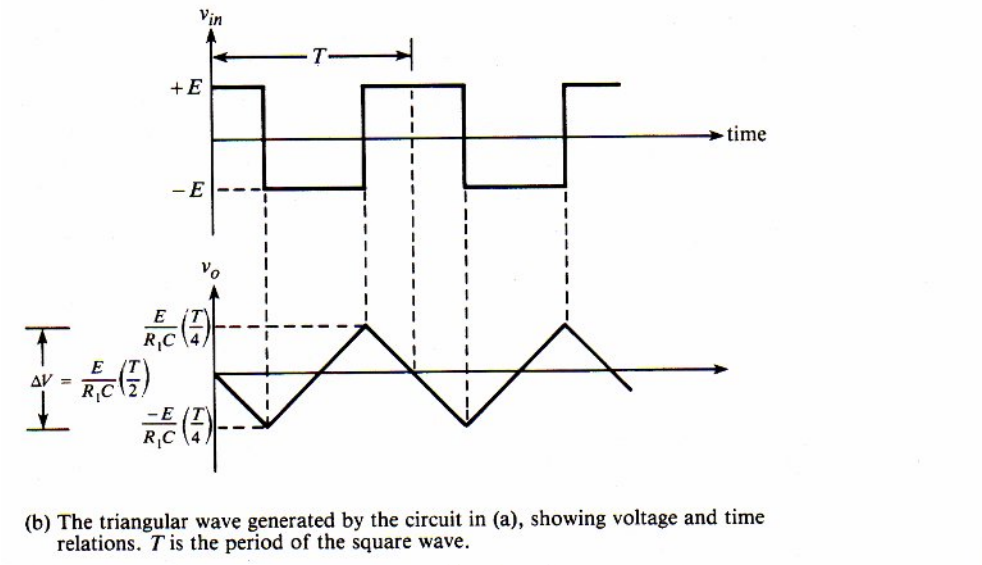


Figure 3-31 The integrator output rises to a maximum of Et_1 while the input is positive, and then falls to 0 at time t_2 when the net area under the input is 0.

The output decreases when the input is positive and increases when the input is negative. The average level (dc component) of the output is 0, assuming no input offset. Note also that the slopes of the triangular wave are ± E/R_1C volts/second, since the integrator gain is $1/R_1C$. It is important to be able to predict these slopes to ensure that they will be within the specified slew rate of the amplifier



(a) Integrator used to generate a triangular waveform



(b) The triangular wave generated by the circuit in (a), showing voltage and time relations. T is the period of the square wave.

Figure 3-32 The practical triangular-waveform generator

T *represents the period of the square wave, the peak value of the triangular wave is*

$$|V_{peak}| = \frac{ET}{4R_1C} \text{ volts} \qquad \text{----------3-64}$$

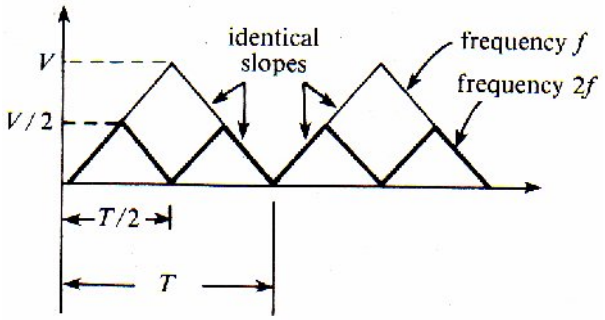


Figure 3-33 When the frequency of the triangular wave produced by an integrator is doubled, the amplitude is halved, so the slopes remain the same.

Equation 3-64 is a special case of a general relationship that can be used to find the integrator's peak output when the input is any periodic waveform symmetric about the horizontal axis:

$$V_{peak} = \frac{\text{positive area in 1/2 cycle of input}}{2R_1C} \qquad \text{----------3-65}$$

Equations 3-64 & 3-65 are based on the assumption that there is no input offset level or dc level in the input waveform. When there is an input dc component, there will be an output dc component given by

$$V_o(\text{dc}) = \frac{-R_f}{R_1} V_{in}(\text{dc}) \qquad \text{----------3-66}$$

Thus, a triangular output will be shifted up or down by an amount equal to V_o(dc).

Example 3-11*. The integrator in Figure 3-34 is to be used to generate a triangular waveform from a 500-Hz square wave connected to its input. Suppose the square wave alternates between ± 12 V*

1. What minimum slew rate should the amplifier have?

2. What maximum output voltage should the amplifier be capable of developing?

3. Repeat (2) if the dc component in the input is -0.2 V. (The square save alternates between + 11.8 V and -12.2 V.)

Solution. *1.The magnitude of the slope of the triangular waveform is*

$$\frac{\Delta V}{\Delta t} = \frac{E}{R_1C} = \frac{12}{400(10^{-6})} = 3 \times 10^4 \text{ V/s}$$

Thus, we must have slew rate $S \geq 3 \times 10^4$ V/s

2. The period T of the 500-Hz square wave is $T = 1/500 = 2 \times 10^{-3}$ s.

$$|V_{peak}| = \frac{ET}{4R_1C} = \frac{12(2 \times 10^{-3})}{4(400)(10^{-6})} = 15 \text{ V}$$

The triangular wave alternates between peak values of + 15 V and -15 V.

3. the dc component in the output is

$$v_o(\text{dc}) = \frac{-R_f}{R_1} V_{in}(\text{dc}) = \frac{-4700}{400}(-0.2) = 2.35 \text{ V}$$

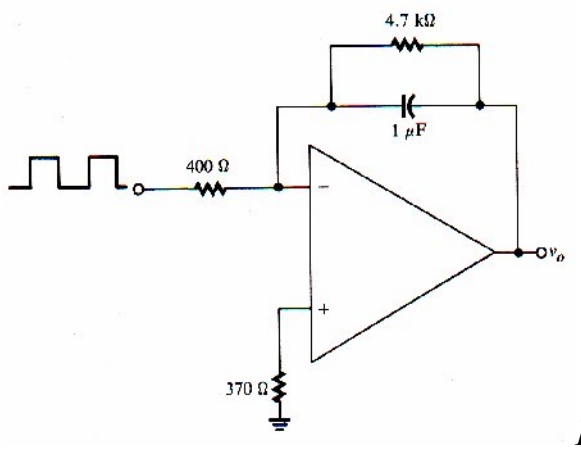


Figure 3-34 (Example 3-11)

Therefore, the triangular output is shifted up by 2.35 V and alternates between peak values of 15 + 2.35 = 17 .35 V and -15 + 2.35 = -12.65 V. The amplifier must be capable of producing a 17.35- V output to avoid distortion.

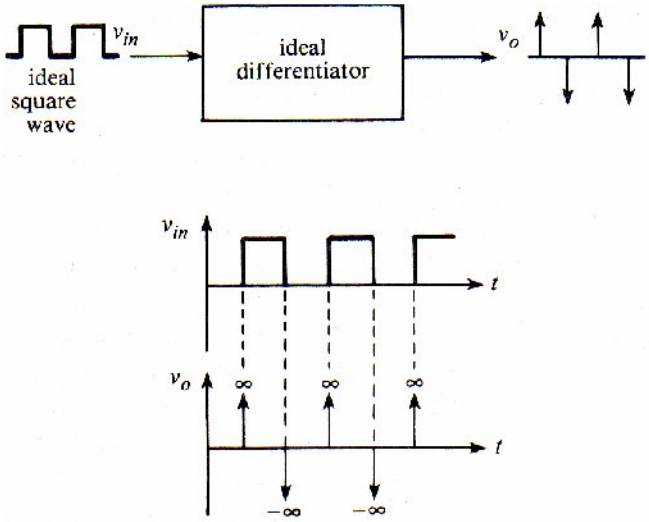


Figure 3-35 The output of an ideal differentiator driven by an ideal square wave is a series of infinite-height, zero-width impulses.

Figure 3-35. illustrated zero-width, infinite-height "spikes" are called impulses. They have zero width because each change in the square wave occurs in zero time, and they have infinite height because the rate of change of the square wave is infinite at the points where changes occur. The negative impulses correspond to the negative rates of change when the square wave goes from a positive value to a negative value. In between the time points where the square wave changes, the rate of change is 0 and so is the output of the differentiator.

The output of a differentiator driven by such a square wave is therefore a series of narrow, high-amplitude pulses.

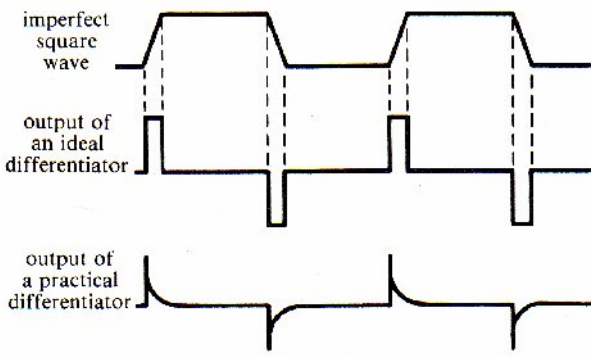


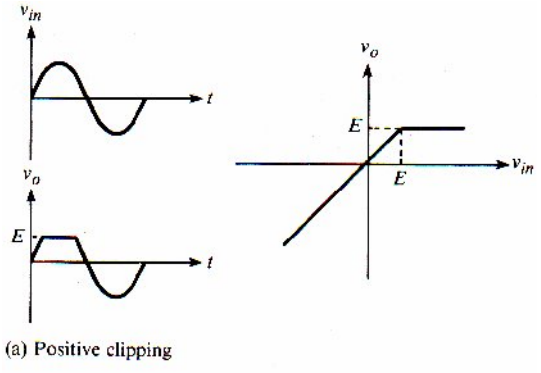
Figure 3-36 Typical outputs from ideal and practical differentiators driven by an imperfect square wave. Phase inversion is not shown.

Figure 3-36 shows a somewhat idealized square wave in which the nonzero rise and fall times are represented by ramps. From Figure 3-36, we deduce that an ideal differentiator driven by a triangular wave will produce a square wave. Since the output equals the rate of change of the input, the square wave will alternate between $\pm (R_f C)\left|\Delta V_o/\Delta_t\right|$ *volts, where* $\Delta V_o/\Delta_t$ *is the rate of change of the triangular input.*

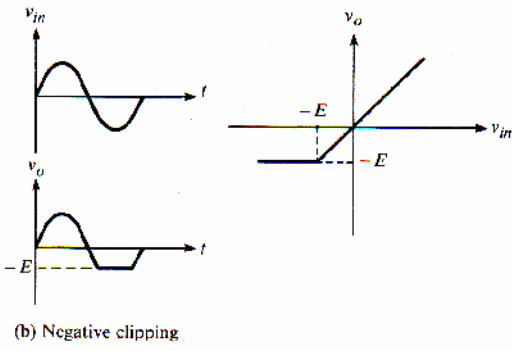
10-Clipping, Clamping , & Rectifying Circuits

10-1 Clipping Circuits

Clipping is the undesirable result of overdriving an amplifier. We have seen that any attempt to push an output voltage beyond the limits through which it can "swing" causes the tops and/or bottoms of a waveform to be "clipped" off, resulting in distortion. Figure 3-68. In each of the examples shown, note that the characteristic becomes horizontal at the output level where clipping occurs. The horizontal line means that the output remains constant regardless of the input level in that region. Outside of the clipping region, the transfer characteristic is simply a line whose slope equals the gain of the device. In these examples, the devices are assumed to have unity gain, so the slope of each line in the linear region is 1.



(a) Positive clipping



(b) Negative clipping

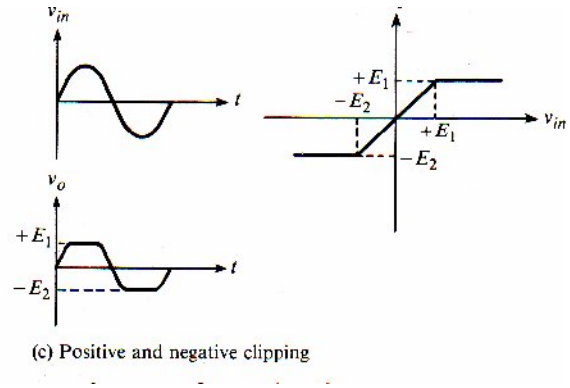


Figure 3-68 Waveform and transfer characteristics of clipping circuits

Figure 3-69 illustrates a somewhat different kind of clipping action. Instead of the positive or negative peaks being "chopped off," the output follows the input when the signal is above or below a certain level.

Clipping can be accomplished using biased diodes, a technique that is more efficient than overdriving an amplifier. Clipping circuits rely on the fact that diodes have very low impedances when they are forward biased and are essentially open circuits when reverse biased.

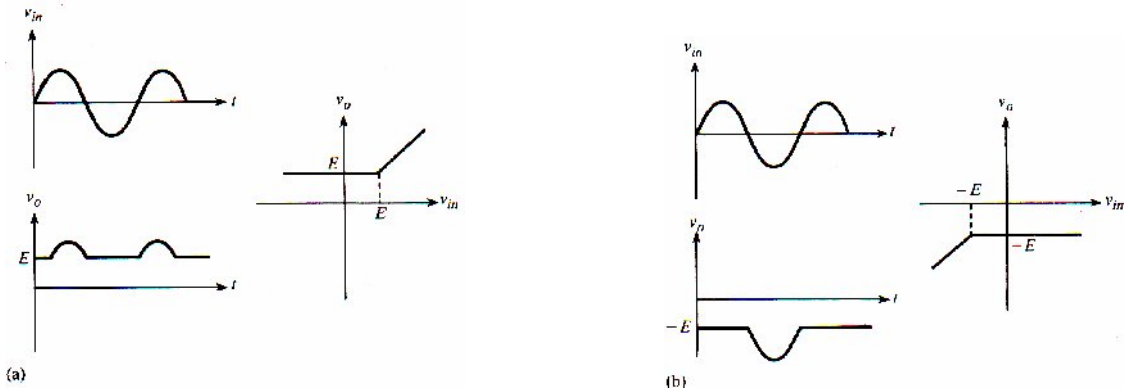
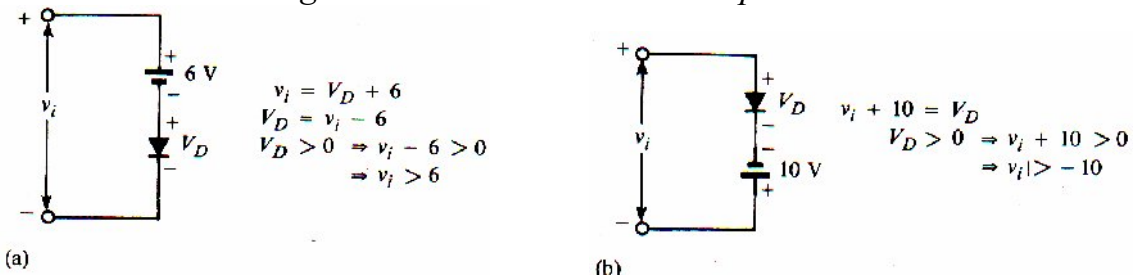


Figure 3-69 Another form of clipping. Compare with Figure 3-68.

If a certain point in a circuit, such as the output of an amplifier, is connected through a very small impedance to a constant voltage, then the voltage at the circuit point differ significantly from the constant voltage. We say in this case that the point is clamped to the fixed voltage. A biased diode is simply a diode connected to a fixed voltage source. The value and polarity of the voltage source determine what value of total voltage across the combination is necessary to forward bias the diode. Figure 3-70 shows several examples.



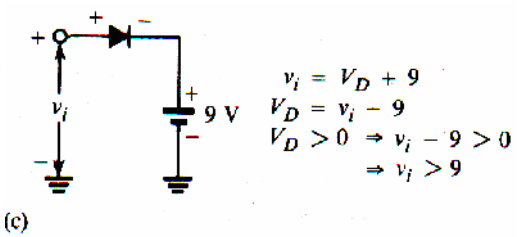


Figure 3-70 Examples of biased diodes and the signal voltages vi required to forward bias them. (Ideal diodes are assumed.) In each case, we solve for the value of vi that is necessary to make V D > 0.

Figure 3-71 shows three examples of clipping circuits using ideal biased diodes and the waveforms that result when each is driven by a sine-wave input. In each case, note that the output equals the dc source voltage when the input reaches the value necessary to forward bias the diode. When the diode is reverse biased by the input signal, it is like an open circuit that disconnects the x source, and the output follows the input. These circuits are called parallel clippers because the biased diode is in parallel with the output.

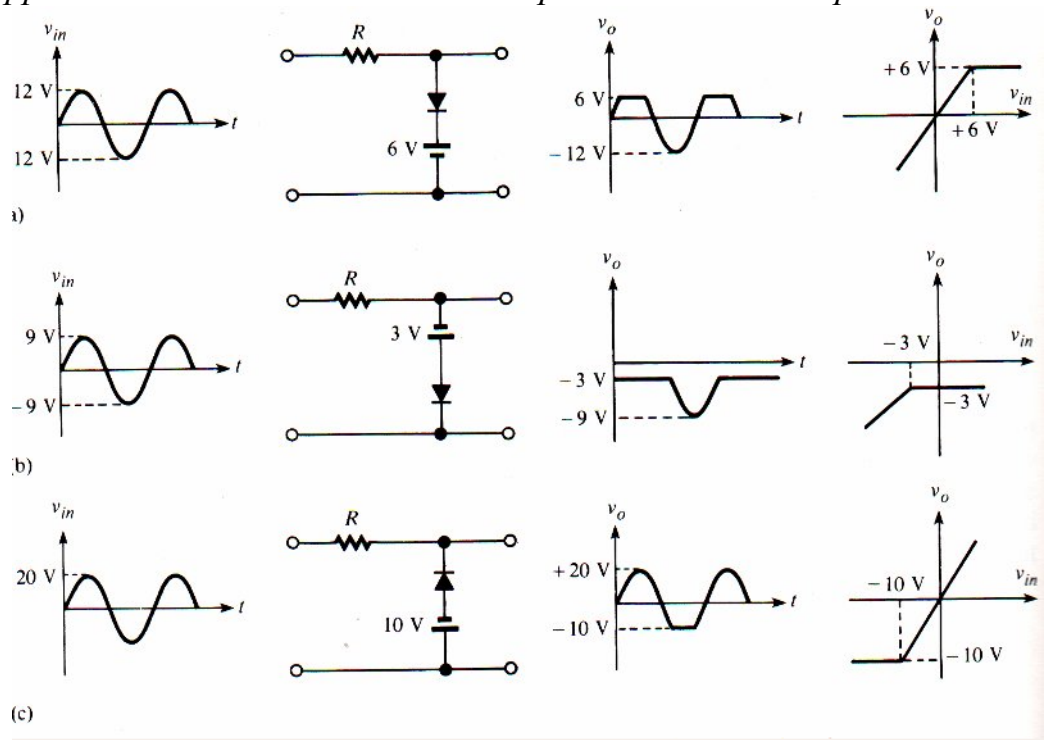


Figure 3-71 Examples of parallel clipping circuits

Figure 3-72(a) shows a biased diode connected in the feedback path of an inverting operational amplifier. The diode is in parallel with the feedback resistor and forms a parallel clipping circuit like that shown in Figure 3-71(a).

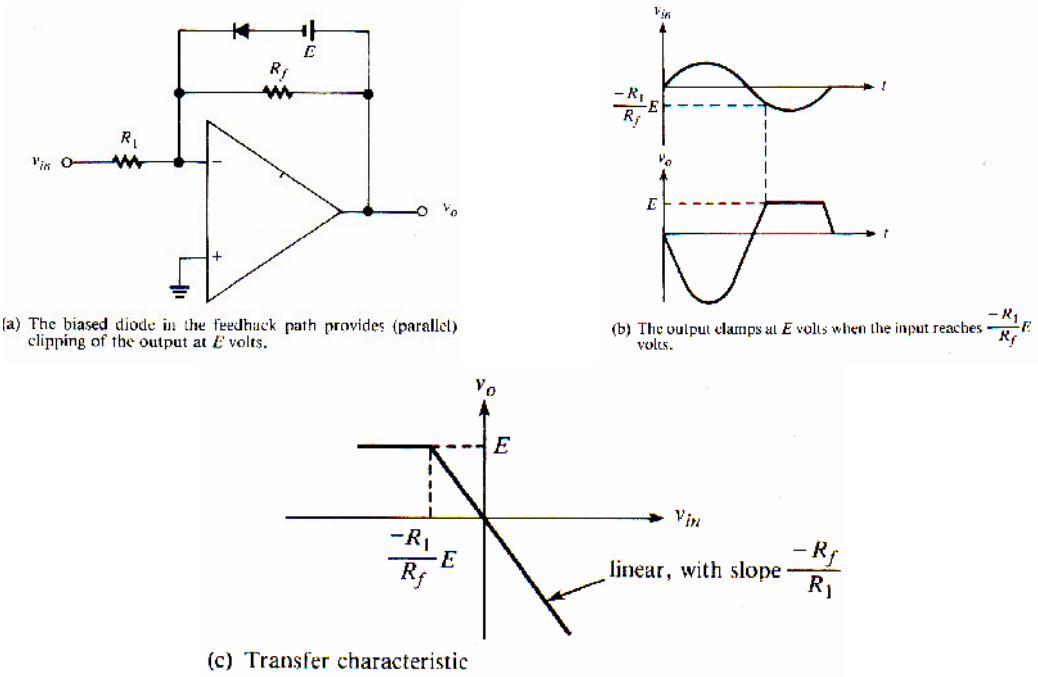


Figure 3-72 An operational-amplifier limiting circuit

Since v- is at virtual ground, the voltage across Rf is the same as the output voltage vo. Therefore, when the output voltage reaches the bias voltage E, the output is held at E volts. Figure 3-72(b) illustrates this fact for a sinusoidal input. Notice that output clipping occurs at input voltage -(R1/Rf)E, since the amplifier inverts and has closed loop gain magnitude Rf/R1. The resulting transfer characteristic is shown in Figure 3-72(c).This circuit is often called a limiting circuit because it limits the output to the dc level clamped by the diode.

Figure 3-73 shows two operational-amplifier clipping circuits using zener diodes. The zener diode conducts like a conventional diode when it is forward biased, so it is necessary to connect a reversed diode in series with it to prevent shorting of Rf When the reverse voltage across the zener diode reaches Vz, the diode breaks down and conducts heavily. while maintaining an essentially constant voltage, Vz, across it. Under those conditions. the total voltage across Rf, i.e., vo = Vz + the forward drop VD, across the conventional diode.

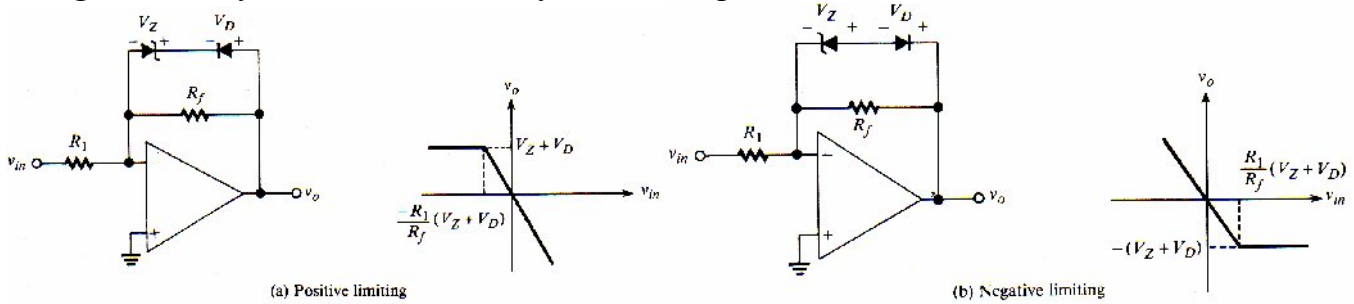


Figure 3-73 Operational-amplifier limiting circuits using zener diodes

Figure 3-74 shows double-ended limiting circuits, in which both positive and negative peaks of the output waveform are clipped. Figure 3-74(a) shows the conventional parallel clipping circuit and (b) shows how double-ended limiting is accomplished in an operational-amplifier circuit. In each circuit, note that no more than one diode is forward biased at any given time, and that both diodes are reverse biased for -E1 < vo < E2, the linear region.

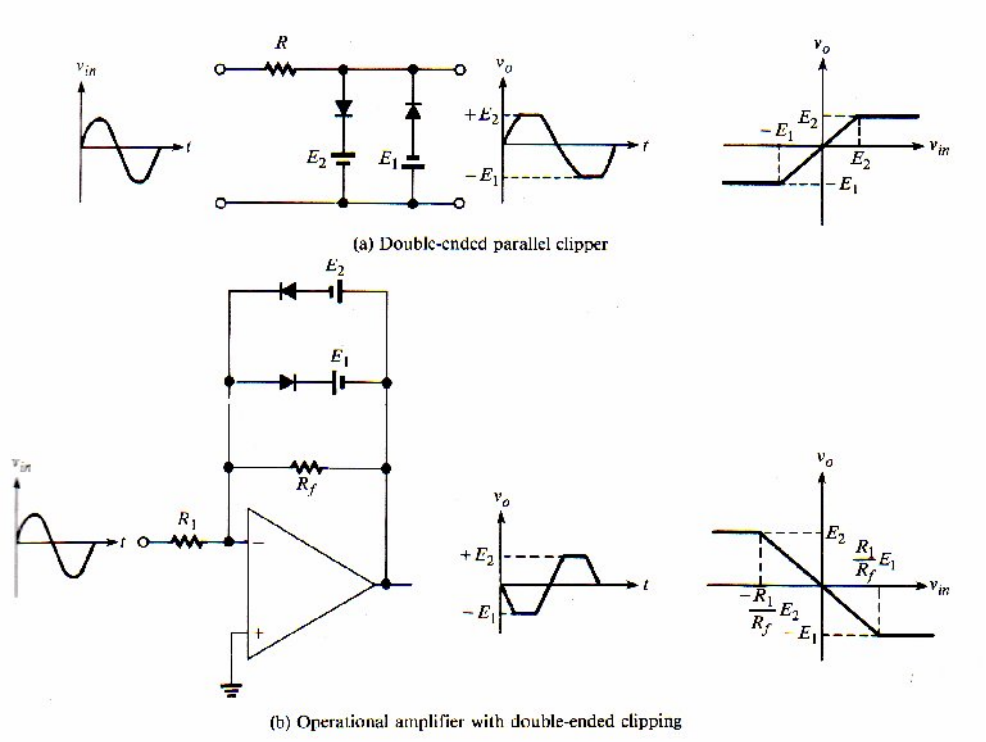


Figure 3-74 Double-ended clipping, or limiting

Figure 3-75 shows a double-ended limiting circuit using back-to-back zener diodes. Operation is similar to that shown in Figure 3-73, but no conventional diode is required. Note that diode D1 is conducting in a forward direction when D2 conducts in its reverse breakdown (zener) region, while D2 is forward biased when D1 is conducting in its reverse breakdown region. Neither diode conducts when -(VZ2 + 0.7) < vo < (VZ1 + 0.7), which is the region of linear amplifier operation.

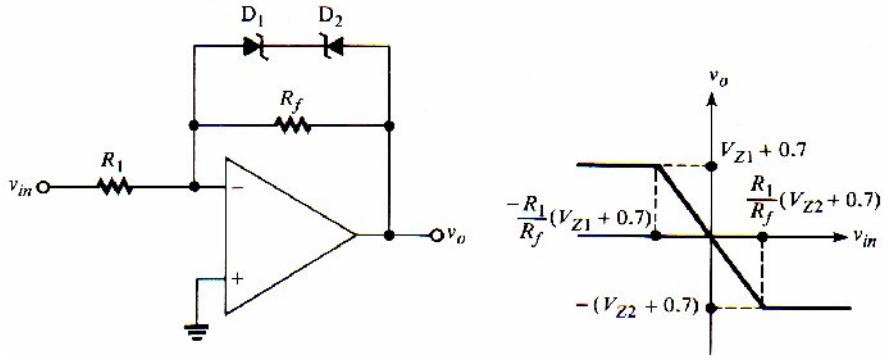


Figure 3-75 A double-ended limiting circuit using zener diodes

10-2 Precision Rectifying Circuits

A rectifier is a device that allows current to pass through it in one direction only. A diode can serve as a rectifier because it permits generous current flow in only one direction-the direction of forward bias.

Rectification is the same as clipping at the zero-volt level: all of the waveform below (or above) the zero-axis is eliminated , however, a diode rectifier has certain intervals of nonconduction, and produces resulting"gaps" at the zero-crossing points of the output

voltage, due to the fact that the input must overcome the diode drop (0.7 V for silicon) before conduction begins.

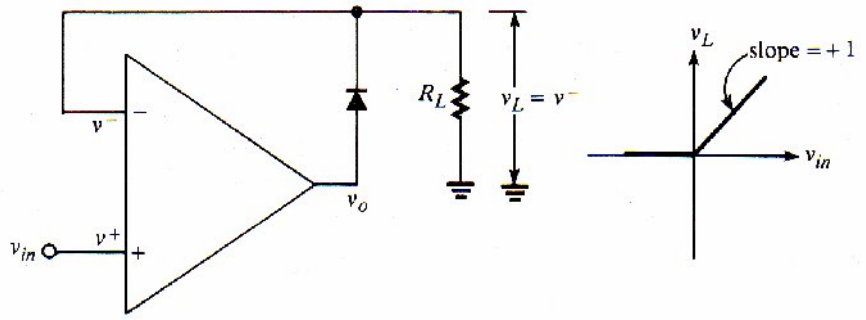


Figure 3-76 A precision rectifier. When vin is positive, the diode is forward biased, and the amplifier behaves like a voltage follower, maintaining $v^+ \approx v^- = vL$.

Figure 3-76 shows one way to obtain precision rectification using an operational amplifier and a diode. The circuit is essentially a noninverting voltage follower when the diode is forward biased. When vin is positive, the output of the amplifier, vo, is positive. the diode is forward biased, and a low-resistance path is established between vo and v-, as necessary for a voltage follower. The load voltage, vL, then follows the positive variations of vin = v^+.
When the input goes negative, vo becomes negative, and the diode is reverse biased. This effectively opens the feedback loop, so vL no longer follows vin The amplifier itself. now operating open-loop, is quickly driven to its maximum negative output, thus holding the diode well into reverse bias.

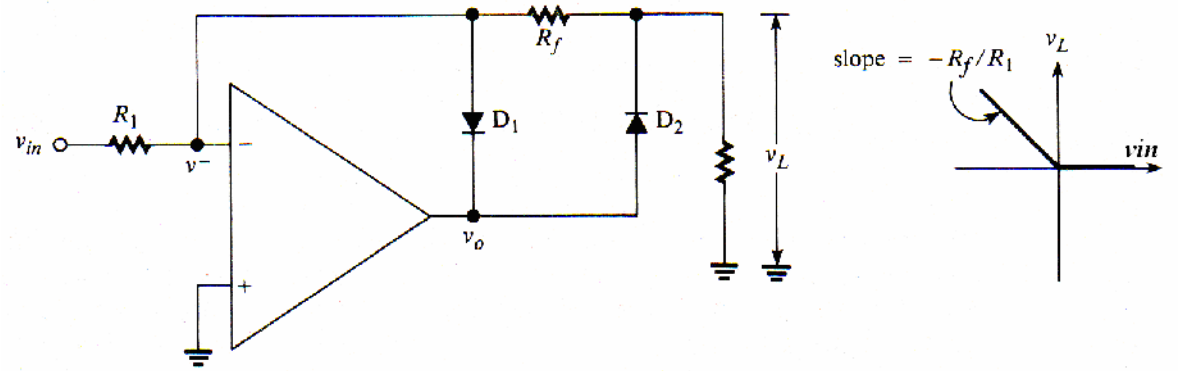


Figure 3-77 A precision rectifier circuit that amplifies and inverts the negative variations in the input voltage

In Figure 3-77. The load voltage is an amplified and inverted version of the negative variations in the input signal. and is 0 when the input is positive. When vin is negative, the amplifier output, vo, is positive, so diode D1 is reverse biased and diode D2 is forward biased. D1 is open and D2 connects the amplifier output through Rf to v^-. Thus, the circuit behaves like an ordinary inverting amplifier with gain –Rf/R1. The load voltage is an amplified and inverted (positive) version of the negative variations in vin , When vin becomes positive,vo is negative, D1 is forward biased, and D2 is reverse biased. D1 shorts the output vo to v^-, which is held at virtual ground, so vL is 0.

10-3 Clamping Circuits

Clamping circuits are used to shift an ac waveform up or down by adding a dc level equal to the positive or negative peak value of the ac signal. Clamping circuits are also called dc level restorers, because they are used in systems (television, for example) where the original dc level is lost in capacitor-coupled amplifier stages. It is important to recognize that the amount of dc-level shift required in these applications varies as the peak value of the ac signal varies over a period of time.

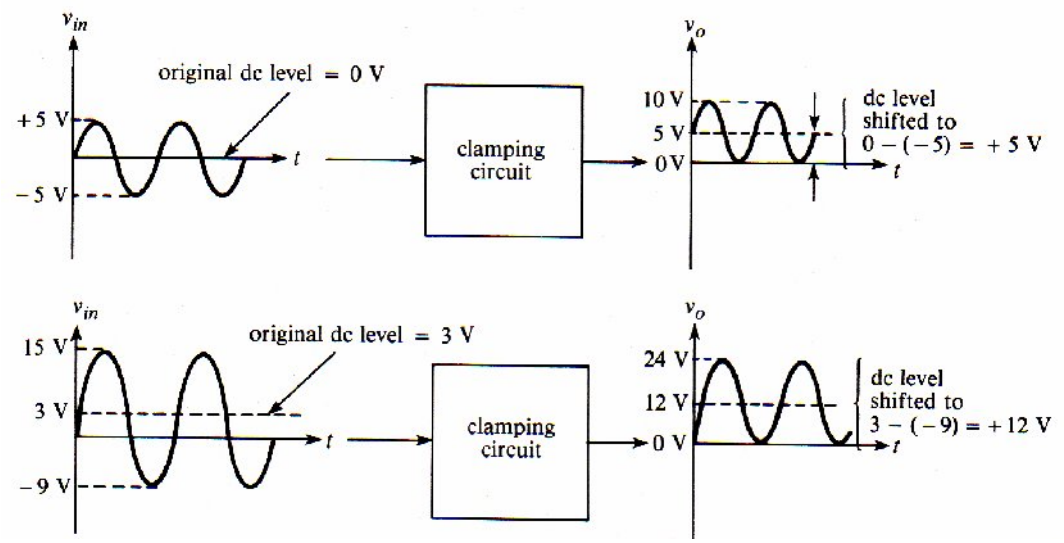


Figure 3-78 clamping circuit that shifts a waveform up by an amount equal to the negative peak value

In Figure 3-78the peak-to-peak value of the output is the same as the peak-to-peak value of the input, and that the output is shifted up by an amount equal to the negative peak of the input

Figure 3-79(a) shows a clamping circuit constructed from passive components. When the input first goes negative, the diode is forward biased, and the capacitor charges rapidly to the peak negative input voltage, V1, The charging time-constant is very small because the forward resistance of the diode is small. Assuming that the capacitor does not discharge appreciably through RL, the total load voltage as vin begins to increase is

$$vL = V1 + vin \quad \text{----------3-120}$$

When the input again reaches its negative peak, the capacitor may have to recharge slightly to make up for any decay that occurred during the cycle. For proper circuit performance, the discharge time-constant, RLC, must be much greater than the period of the input.

If the diode connections are reversed, the waveform is shifted down by an amount equal to the positive peak voltage, V2. If the diode is biased by a fixed voltage, the waveform can be shifted up or down by an amount equal to a peak value plus or minus the bias voltage.

Figure 3-79(b) shows the load voltage that results if the diode is assumed to have zero voltage drop. In reality, since the capacitor charges through the diode, the voltage across the capacitor only reaches V1 minus the diode drop. Consequently,

$$vL = vin + V1 - 0.7 \text{ -------3-121}$$

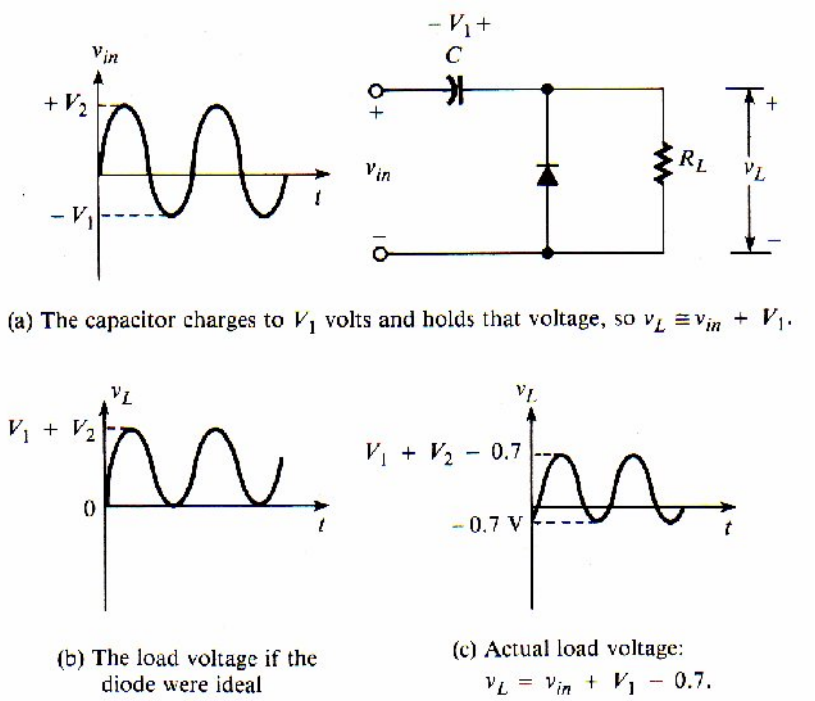


Figure 3-79 A clamping circuit consisting of a diode and a capacitor

The waveform that results is shown in Figure 3-79(c).
If precision clamping is required, the operational-amplifier circuit shown in Figure 3-80 can be used. When vin in Figure 3-80 first goes negative, the amplifier output, vo. is positive and the diode is forward biased. The capacitor quickly charges to V1, with the polarity shown. Notice that vL = Vin + V1 and that the drop across the diode does not appear in vL. With the capacitor voltage having the polarity shown, v- becomes positive. and remains positive throughout the cycle, so the amplifier output is negative. Therefore. the diode is reverse biased and the feedback loop is opened. The amplifier is driven to its maximum negative output level and the diode remains reverse biased. During one cycle of the input, the capacitor may discharge somewhat into the load, causing its voltage to fall below V1. If so, then when vin once again reaches its maximum negative voltage, v- will once again be negative, vo will be positive, and the capacitor will be allowed to recharge to V1 volts, as before.

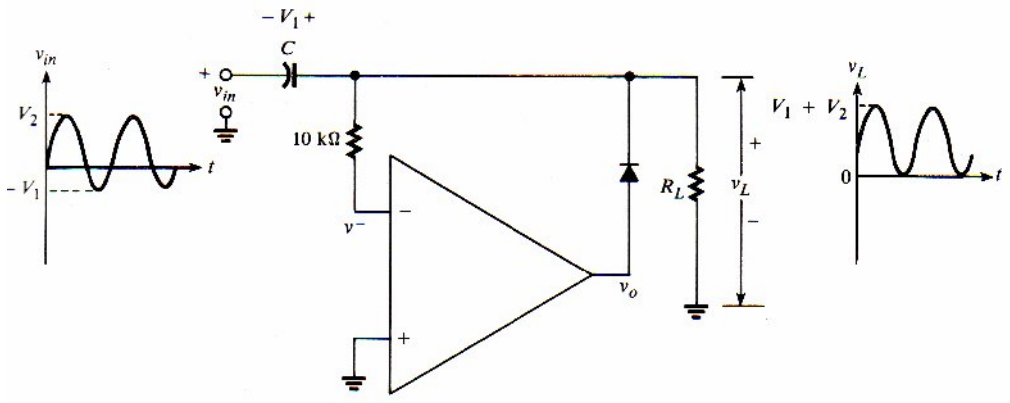


Figure 3-80 A precision clamping circuit

4-Integrated Circuit Power Amplifiers

A power amplifier is one that is designed to deliver a large amount of power to a load. To perform this function, a power amplifier must itself be capable dissipating large amounts of power; so that the heat generated when it is operated at high current and voltage levels is released into the surroundings at a rate fast enough to prevent destructive temperature build-up. power amplifiers typically contain bulky components having large surface areas to enhance heat transfer to the environment.

A power transistor is a discrete device with a large surface area and a metal case .A power amplifier is often the last stage of an amplifier system designed to modify signal characteristics referred to as signal conditioning.

it is designed at least one of its semiconductor components, typically a power transistor, can be operated over substantially the entire range of its output characteristics, from saturation to cutoff. This mode of operation is called large-signal operation.

The term "large-signal operation" is also applied to devices used in digital switching circuits. In these applications, the output level switches between "high" and "low" (cutoff and saturation), but remains in those states most of the time. Signal distortion occurs because of the change in amplifier characteristics with signal level.

4-1 Transistor power dissipation

power is, the rate at which energy is consumed or dissipated (1 watt = 1 joule/second).

If the rate at which heat energy is dissipated in a device is less than the rate at which it is generated, the temperature of the device must rise. In electronic devices, electrical energy is converted to heat energy at a rate given by P = VI watts, and temperature rises when this heat energy is not removed at a comparable rate.

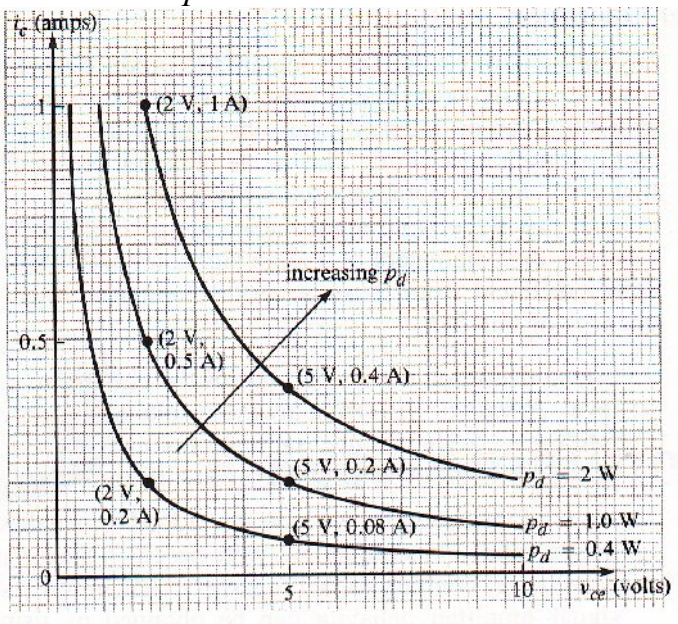


Figure 4-1 A family of graphs (hyperbolas) corresponding to Pd = Vce x ic for different values of Pd. Each hyperbola represents all combinations of collector voltage and collector current that result in a specific power dissipation (value of Pd)

Since semiconductor material is irreversibly damaged when subjected to temperatures beyond a certain limit, temperature is the parameter that ultimately limits the amount of power a semiconductor device can handle. Transistor manufacturers specify the maximum permissible junction temperature and the maximum permissible power dissipation that a transistor can withstand. Most of the heat generated in a transistor is produced at the collector-base junction. The total power dissipated at the junctions is

$$p_d = v_{cb}i_c + v_{be}i_e \approx (v_{cb} + v_{be})i_c = v_{ce}i_c \quad \text{----------4-1}$$

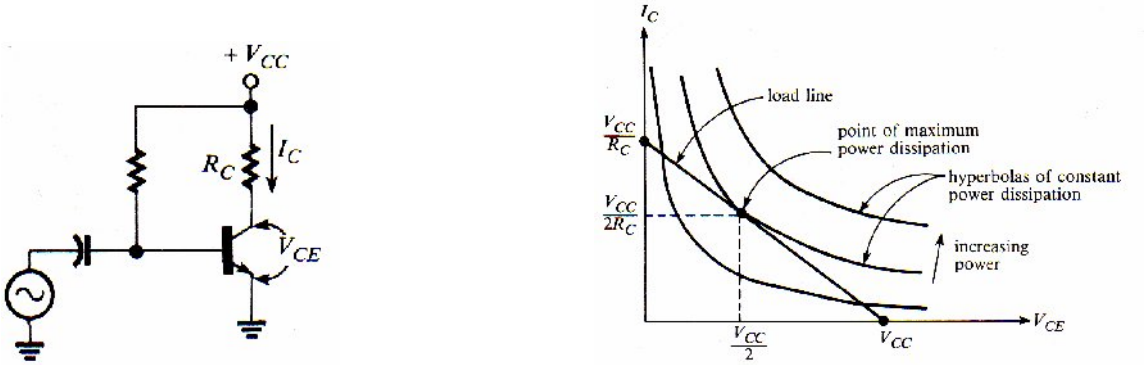


Figure 4-2 load lines and hyperbolas of constant power dissipation

As the amplifier output changes in response to an input signal, the collector current and voltage undergo variations along the load line must lie below and to the left of the hyperbola corresponding to the maximum permissible power dissipation. It can be shown that the point of maximum power dissipation occurs at the center of the load line, where VCE = Vcc/2 and Ic = Vcc/2Rc . Therefore, the maximum power dissipation is

$$p_d(\max) = \left(\frac{V_{CC}}{2}\right)\left(\frac{V_{CC}}{2R_C}\right) = \frac{V_{CC}^2}{4R_C} \quad \text{----------4-2}$$

Therefore we require that

$$\frac{V_{CC}^2}{4R_C} < P_d(\max) \quad \text{----------4-3}$$

Pd(max) the manufacturer's specified maximum dissipation at a specified ambient temperature.

$$R_C > \frac{V_{CC}^2}{4P_d(\max)} \quad \text{----------4-4}$$

Example 4-1. *The amplifier in Figure 4-2 is to be operated with Vcc=20V and Rc=1 kΩ.*
1. What maximum power dissipation rating should the transistor have?
2. If an increase in ambient temperature reduces the maximum rating found in (1) by a factor of 2, what new value of Rc should be used to ensure safe operation?
Solution.*1.*

$$P_d(\max) > \frac{V_{CC}^2}{4R_C} = \frac{(20)^2}{4(10^3)} = 0.1 \text{ W}$$

2. When the dissipation rating is decreased to 0.05W the maximum permissible value of Rc is

$$R_C > \frac{V_{CC}^2}{4P_d(\max)} = \frac{(20)^2}{4(0.05)} = 2 \text{ k}\Omega$$

4-5 AMLIFIER CLASSES AND EFFICIENCY

4-5-1 Class-A Amplifiers

All the small-signal amplifiers have been designed so that output voltage can vary in response to both positive and negative inputs; that is, the amplifiers are biased so that under normal operation the output never saturates or cuts off. An amplifier that has that property is called a class-A amplifier(its output remains in the active region during a complete cycle (one full period) of a sine-wave input signal).

Figure 4-5 The output of a class-A amplifier remains in the active region during a full period (360°) of the input sine wave. In this example, the transistor output is biased midway between saturation and cutoff. In this case, the transistor is biased at VCE = V cc/2, which is midway between saturation and cutoff, and which permits maximum output voltage swing. Note that the output can vary through a full Vcc volts, peak-to-peak.

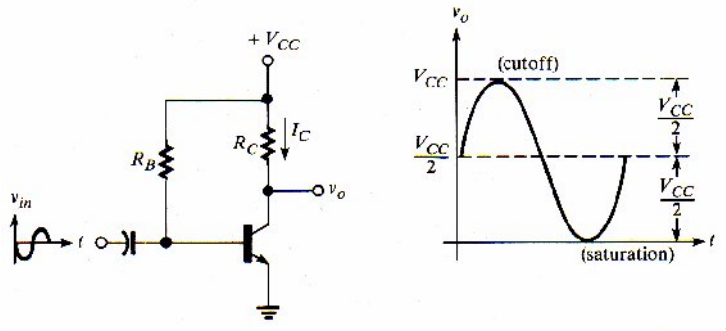


Figure 4-5

Efficiency

The efficiency of a power amplifier is defined to be

$$\eta = \frac{\text{average signal power delivered to load}}{\text{average power drawn from dc source(s)}} \text{ ----------4-9}$$

Note that the numerator of (4-9) is average ac power, excluding any dc or bias components in the load. Recall that when voltages and currents are sinusoidal, average ac power can be calculated using any of the following relations:

$$P = V_{rms}I_{rms} = V_P I_P/2 = V_{PP}I_{PP}/8 \text{ ----------4-10}$$

$$P = I^2_{rms}R = I^2_P R/2 = I^2_{PP}R/8 \text{ ----------4-11}$$

$$P = V^2_{rms}/R = V^2_P/2R = V^2_{PP}/8R \text{ ----------4-12}$$

The efficiency of a class-A amplifier is 0 when no signal is present. (The amplifier is said to be in standby). To derive a general expression for the efficiency of the class-A amplifier shown in Figure 4-5, we will not consider the small power consumed in the base-biasing circuit, i.e., the power at the input side $I^2_B R_B$ + vbe ib.

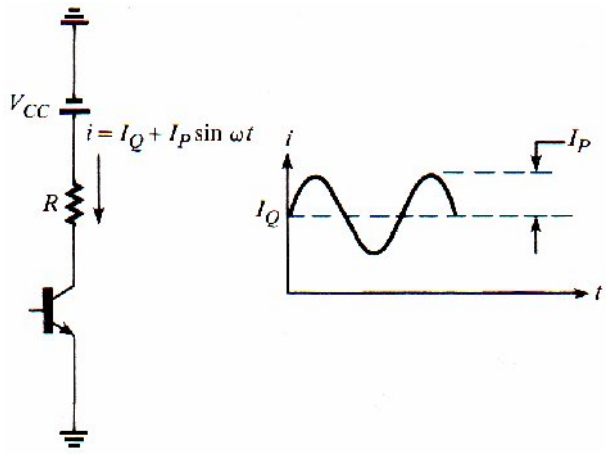


Figure 4-6 Voltages and currents used in the derivation of an expression for the efficiency of a series-fed, class-A amplifier

R is the load. Referring to this configuration as a series-fed class-A amplifier
The instantaneous power from the dc supply is

$$p_S(t) = V_{CC}i = V_{CC}(I_Q + I_P \sin \omega t) = V_{CC}I_Q + V_{CC}I_P \sin \omega t \quad \text{----------4-13}$$

Since the average value of the sine term is 0, the average power from the dc supply is

$$P_S = V_{CC}I_Q \text{ watts} \quad \text{----------4-14}$$

The average signal power in load resistor R is, from equation 4-11,

$$P_R = I_P^2 R/2 \text{ watts} \quad \text{----------4-15}$$

Therefore, by equation 4-9

$$\eta = \frac{P_R}{P_S} = \frac{I_P^2 R}{2V_{CC}I_Q} \quad \text{----------4-16}$$

The efficiency is 0 under no-signal conditions (Ip = 0) and that efficiency rises as the peak signal level Ip increases. The maximum possible efficiency occurs when Ip has its maximum possible value without distortion. When the bias point is at the center of the load line(Fig 4-2), the quiescent current is one-half the saturation current, and the output current can swing through the full range from 0 to Vcc/R amps without distorting. Thus, the maximum undistorted peak current is also one-half the saturation current:

$$I_Q = I_P(\max) = V_{CC}/2R \quad \text{----------4-17}$$

Substituting (4-17) into (4-16), we find the maximum possible efficiency of the series-fed, class-A amplifier:

$$\eta(\max) = \frac{(V_{CC}/2R)^2 R}{2V_{CC}(V_{CC}/2R)} = 0.25 \quad \text{---------4-18}$$

This result shows that the best possible efficiency of a series-fed, class-A amplifier is undesirably small: only 1/4 of the total power consumed by the circuit is delivered to the load, under optimum conditions. For that reason, this type of amplifier is not widely used in heavy power applications. The principal advantage of the class-A amplifier is that it generally produces less signal distortion than some of the other, more efficient classes that we will consider later.

Another type of efficiency relates signal power to total power dissipated at the collector. Called collector efficiency, it is desirable to maximize the ratio of signal power in the load to power consumed by the device. Collector efficiency ήc is defined by

$$\eta_c = \frac{\text{average signal power delivered to load}}{\text{average power dissipated at collector}} \quad \text{----------4-19}$$

The average power Pc dissipated at the collector of the class-A amplifier in Figure 4-6 is the product of the dc (quiescent) voltage and current:

$$P_C = V_Q I_Q = (V_{CC} - I_Q R) I_Q \quad \text{----------4-20}$$

$$\eta_c = \frac{I_p^2 R/2}{(V_{CC} - I_Q R) I_Q} \quad \text{----------4-21}$$

The maximum value of η_c occurs when Ip is maximum, Ip = I_Q = Vcc/2R. Substituting these values into (4-21) gives

$$\eta_c(\max) = \frac{(V_{CC}/2R)^2 R/2}{(V_{CC} - V_{CC}/2)V_{CC}/2R} = 0.5 \quad \text{----------4-22}$$

The average power delivered to the load is

$$P_L = I_{PL}^2 R_L/2 \quad \text{----------4-23}$$

where I_{PL} is the peak ac load current.
The average power from the dc source is computed in the same way as for the series-fed amplifier: P_S = VccI_Q, so the efficiency is

$$\eta = \frac{I_{PL}^2 R_L}{2V_{CC} I_Q} \quad \text{----------4-24}$$

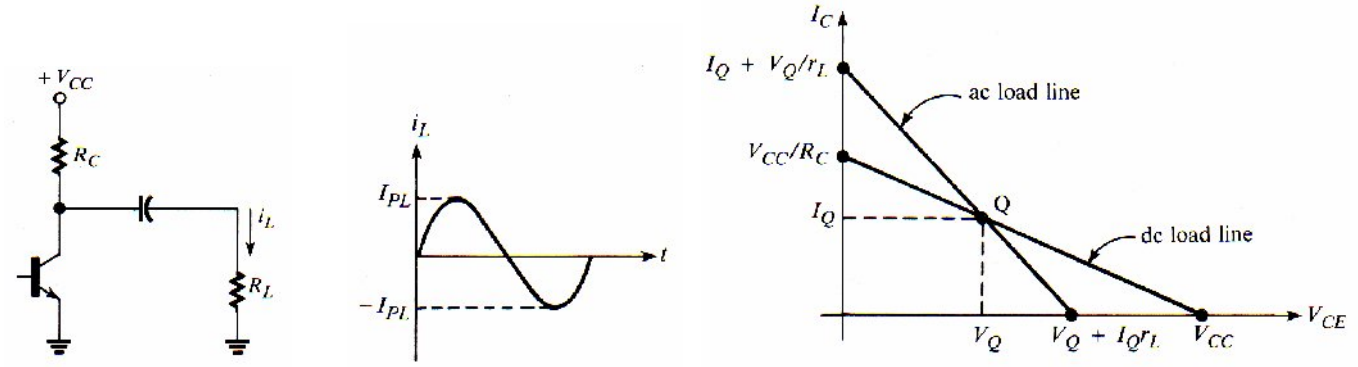


Figure 4-7 A class-A amplifier with capacitor-coupled load RL

The efficiency is 0 under no-signal (standby) conditions and increases with load current I_{PL}. maximum output swing can be achieved by setting the Q-point in the center of the ac load line, at

$$I_Q = \frac{V_{CC}}{R_C + r_L} \quad \text{----------4-25}$$

The peak collector current under those circumstances is Vcc/(Rc+r_L). Neglecting the transistor output resistance, the portion of the collector current that flows in R_L is, by the current-divider rule,

$$I_{PL} = \left(\frac{V_{CC}}{R_C + r_L}\right)\left(\frac{R_C}{R_C + R_L}\right) \text{----------4-26}$$

average ac power in the load resistance R_L is then

$$P_L = \frac{I_{PL}^2 R_L}{2} = \left[\left(\frac{V_{CC}}{R_C + r_L}\right)\left(\frac{R_C}{R_C + R_L}\right)\right]^2 (R_L/2) \text{----------4-27}$$

The average power supplied from the dc source is

$$P_S = V_{CC} I_Q = \frac{V_{CC}^2}{R_C + r_L} \text{----------4-28}$$

Therefore, the efficiency under the conditions of maximum possible undistorted output is

$$\eta = \frac{P_L}{P_S} = \frac{\left[\left(\frac{V_{CC}}{R_C + r_L}\right)\left(\frac{R_C}{R_C + R_L}\right)\right]^2 R_L}{2\left(\frac{V_{CC}^2}{R_C + r_L}\right)} \text{----------4-29}$$

Algebraic simplification of (4-29) leads to

$$\eta = \frac{R_C R_L}{2(R_C + 2R_L)(R_C + R_L)} = \frac{r_L}{2(R_C + 2R_L)} \text{----------4-30}$$

the efficiency depends on both Rc and R_L. In practice, R_L is a fixed and known value of load resistance, while the value of Rc is selected by the designer. Using calculus (differentiating equation 4-30 with respect to Rc), it can be shown that ή is maximized by setting

$$R_C = \sqrt{2} R_L \text{----------4-31}$$

With this value of R_C, the maximum efficiency is

$$\eta(\text{max}) = 0.0858 \text{----------4-32}$$

Another criterion for choosing Rc is to select its value so that maximum power is transferred to the load, maximum power transfer occurs when $R_C = R_L = R$. Under that circumstance, $r_L = R/2$, and, by substituting into (4-30), we find the maximum possible efficiency with maximum power transfer to be

$$\eta(\text{max}) = 0.0833 \quad (\text{max power transfer}) \text{----------4-33}$$

the efficiency under maximum power transfer (0.0833) is somewhat less than that which can be achieved (0.0858) without regard to power transfer. In either case, the maximum efficiency is substantially less than that attainable in the series-fed class-A amplifier.

Example 4-5: *The class- A amplifier shown in Figure 4-8 is biased at VCE = 12 V. The out put voltage is the maximum possible without distortion. Find*

1. the average power from the dc supply
2. the average power delivered to the load
3. the efficiency:
4. the collector efficiency

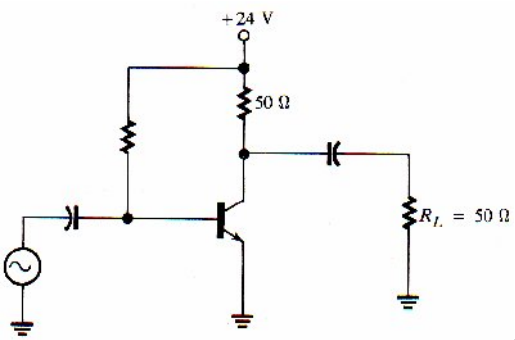


Figure 4-8(Example 4-5)

Solution:

$$1.\ I_Q = (V_{CC} - V_Q)/R_C = (24 - 12)/50 = 0.24\ \text{A}$$
$$P_S = V_{CC}I_Q = (24\ \text{V})(0.24\ \text{A}) = 5.76\ \text{W}$$

2. As in Fig 4-7 the maximum value of the peak output voltage is the smaller of V_Q and $I_Q r_L$. In this case, V_Q = 12V and $I_Q r_L$ = (0.24A)(50 ‖ 50) = 6V Thus, the peak undistorted output voltage is 6V and the ac power delivered to the 50-Ω load is

$$P_L = \frac{V_{PL}^2}{2R_L} = \frac{6^2}{100} = 0.36\ \text{W}$$

3.

$$\eta = \frac{P_L}{P_S} = \frac{0.36}{5.76} = 0.0625$$

The efficiency is less than the theoretical maximum because the bias point permits only a ± 6V swing.

4. The average power dissipated at the collector is $Pc=V_QI_Q$= (12)(0.24) = 2.88W. Therefore,

$$\eta_c = \frac{P_L}{P_C} = \frac{0.36}{2.88} = 0.125$$

4-5-1-2Transformer-coupled Class-A Amplifiers

Transformers used to couple power amplifiers to their loads in those applications called output transformers. the advantages of a transformer is to achieve impedance matching for maximum power transfer and that it blocks the flow of dc current in a load.

Fig 4-9 shows a transformer used to couple the output of a transistor to load RL. Also shown the dc and ac load lines for the amplifier. we assume the dc resistance of the primary winding is negligibly small, so the dc load line is vertical (slope = $-1/R_{dc}$= -∞). the ac resistance r_L reflected to the primary side is

$$r_L = (N_P/N_S)^2\ R_L \quad \text{----------4-34}$$

N_P & N_S the numbers of turns on the primary & secondary windings, the slope of the ac load line is $-1/ r_L$.

Since we are assume to negligible resistance in the primary winding, there is no dc voltage drop across the winding, and the quiescent collector voltage is therefore V_{CC} volts(V_Q= V_{CC}). Since V_{CE} cannot be negative, the maximum permissible decrease in V_{CE} below the quiescent value is V_Q= V_{CC} volts. Thus, the maximum possible peak value of V_{CE} is V_{CC} volts($V_{CE(max)}$=V_{CC}) . To achieve maximum peak-to-peak output variation, the intercept of the ac load line on the V_{CE}-axis should therefore be $2V_{CC}$ volts. The quiescent current I_Q is selected so that the ac load line intersects the V_{CE} -axis at $2V_{CC}$ volts.

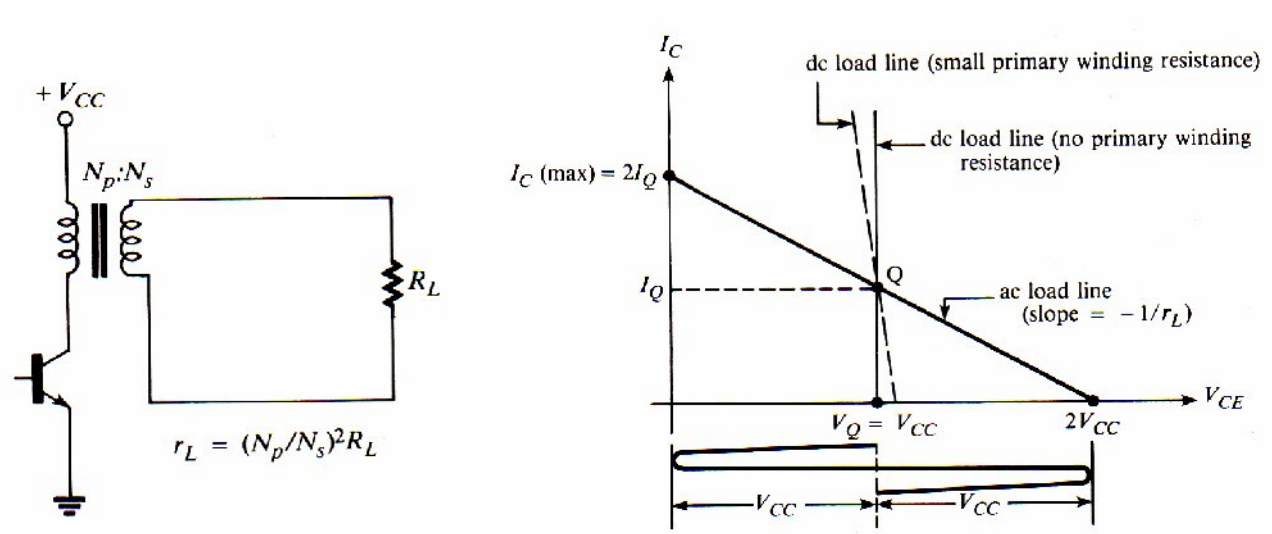


Figure 4-9 Transformer-coupled, class-A amplifier and load lines. The amplifier is biased for maximum peak-to-peak variation in V_{CE}

The ac load line intersects the I_C - axis in at $I_{C(max)}$.
When I_Q is set for maximum signal swing ($V_{CE(max)} = 2V_{CC}$), $I_Q = 1/2\ I_{C(max)}$; $I_{C(max)} = 2I_Q$. Thus, the maximum values of the peak primary voltage and peak primary current are V_{CC} and I_Q . Since the ac output can vary through this range, below and above the quiescent point, the amplifier is of the class-A type.
unlike the case of the capacitor-coupled or series-fed amplifier, the collector voltage can exceed the supply voltage.
The ac power delivered to load resistance R_L in Fig4-9 is

$$P_L = \frac{V_s^2}{2R_L} = \frac{V_{PL}^2}{2R_L} \text{ watts} \quad \text{----------4-35}$$

$V_S = V_{PL}$ is the peak value of the secondary, or load, voltage. The average power from the dc supply is

$$P_S = V_{CC} I_Q \text{ watts} \quad \text{----------4-36}$$

Therefore, the efficiency is

$$\eta = \frac{P_L}{P_{S9}} = \frac{V_{PL}^2}{2R_L V_{CC} I_Q} \quad \text{----------4-37}$$

at maximum signal conditions, the peak primary voltage is V_{CC} volts, so the peak load voltage

$$V_{PL} = (N_s/N_p) V_{CC} \quad \text{----------4-38}$$

Also, since the slope of the ac load line is $-1/r_L$, we have

$$\frac{|\Delta I_C|}{|\Delta V_{CE}|} = \frac{1}{r_L} = \frac{I_Q}{V_Q}$$

Or

$$I_Q = \frac{V_Q}{r_L} = \frac{V_{CC}}{(N_p/N_s)^2 R_L} \quad \text{----------4-39}$$

The maximum possible efficiency of the class-A, transformer-coupled amplifier:

$$\eta(\max) = \frac{(N_s/N_p)^2 V_{CC}^2}{(2R_L V_{CC})\dfrac{V_{CC}}{(N_p/N_s)^2 R_L}} = 0.5 \quad \text{----------4-40}$$

the maximum efficiency is twice that of the series-fed class-A amplifier and six times that of the capacitor-coupled class-A amplifier. This improvement in efficiency is attributable to the absence of external collector resistance that would otherwise consume dc power. The average power from the dc supply is the same as the collector dissipation:

$$P_S = V_{CC} I_Q = V_Q I_Q = P_C \text{ ----------4-41}$$

In practice, a full output voltage swing of $2V_{CC}$ volts cannot be achieved in a power transistor. The device is prevented from cutting off entirely and it cannot be driven all the way into saturation ($Ic = I_{C(max)}$)without creating excessive distortion. These points are illustrated in the next example.

Example 4-6: *The transistor in the power amplifier shown in Fig4-10 has the output characteristics shown in Fig4-11. Assume that the transformer has zero resistance.*

1. Construct the (ideal) dc and ac load lines necessary to achieve maximum output voltage swing. What quiescent values of collector and base current are necessary to realize the ac load line?

2. What is the smallest value of $I_{C(max)}$ for which the transistor should be rated?

3. What is the maximum peak-to-peak collector voltage, and what peak-to-peak base current is required to achieve it? Assume that the base current cannot go negative and that, to minimize distortion, the collector should not be driven below 2.5 V in the saturation region.

4. Find the average power delivered to the load under the maximum signal conditions of (3).

5. Find the power dissipated in the transistor under no-signal conditions (standby).

6. Find the efficiency.

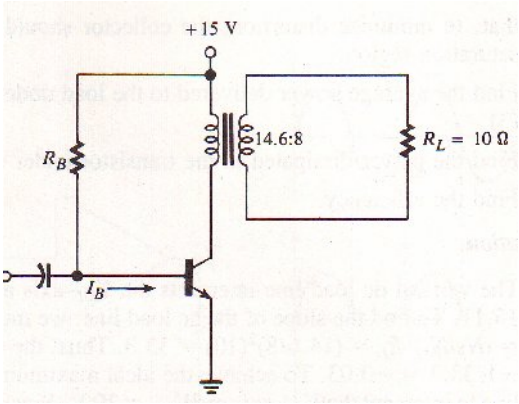


Fig4-10 Example (4-6)

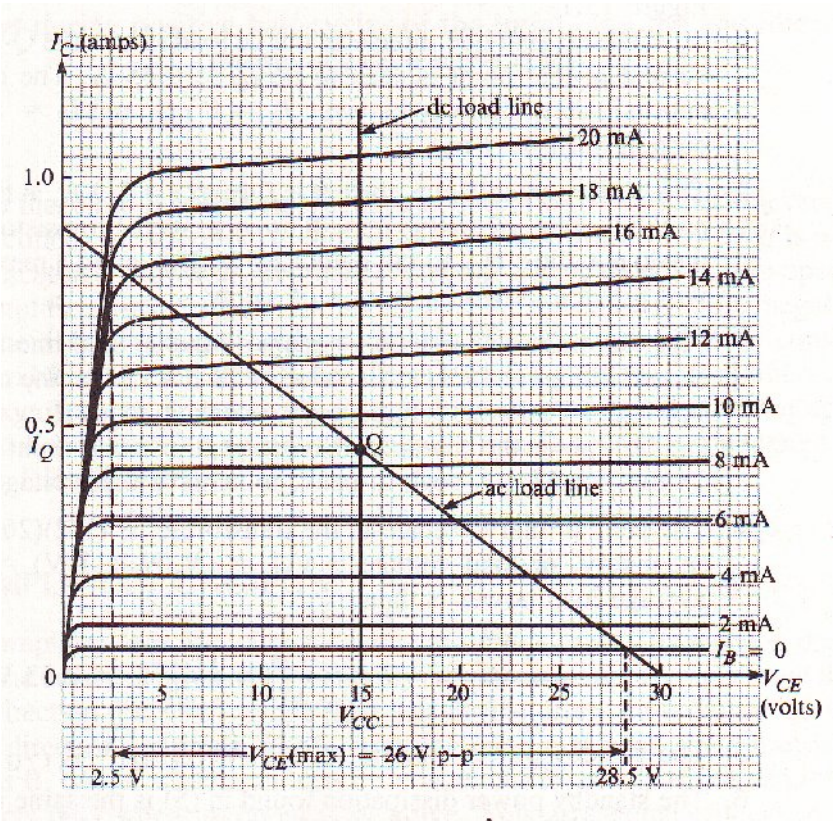


fig4-11 Example(4-6)

Solution:

1. *The vertical dc load line intersects the V_{CE}-axis at V_{CC}= 15Vas shown in fig4-11 . To find the slope of the ac load line, we must find r_L.*

$r_L = (Np/N_S)^2 R_L = (14.6/8)^2(10) = 33.3\Omega$. Thus, the slope of the ac load line is -1/ r_L = -1/33.3 = -0.03 A/V. To achieve the ideal maximum output swing, we want the ac load line to intercept the V_{CE}-axis at $2V_{CC}$ = 30 V. Since the slope of that line has magnitude 0.03, it will intercept the I_C-axis at I_C = (0.03 A/V)(30 V) = 0.9 A. The ac load line 15 then drawn between the two intercepts (0 A, 30 V) & (0.9 A, 0 V), as shown in Fig 4-11.

The ac load line intersects the dc load line at the Q-point. The quiescent collector current at that point is seen to be I_Q= 0.45 A. The corresponding base current I_B approximately halfway between I_B = 8 mA & I_B = 10 mA, so the quiescent base current must be 9 mA.

2. The maximum collector current is $I_{C(max)}$ = 0.9 A, at the intercept of the ac load line on the I_C-axis. Actually, we will not operate the transistor that far into saturation, since we do not allow V_{CE} to fall below 2.5 V. However, a maximum rating of 0.9 A (or 1A) will provide us with a margin of safety.

3. The maximum value of V_{CE} occurs on the ac load line at the point where I_B = 0 as shown in Fig 4-11, this value is 28.5 V. Since the minimum permissible value of V_{CE} is 2.5 V, the maximum peak-to-peak voltage swing is 28.5 - 2.5 = 26 Vp-p. As can be seen on the characteristic curves, the base current must vary from I_B = 0 to I_B =18 mA, or 18 mA peak-to-peak, to achieve that voltage swing.

4. The peak primary voltage in the transformer is (1/2)(26) = 13 V. Therefore the peak secondary, or load voltage is $V_{PL} = (N_S/N_p)(13\ V) = (8/14.6)13 = 7.12\ V$. The average load power is then

$$P_L = \frac{V_{PL}^2}{2R_L} = \frac{(7.12)^2}{20} = 2.53\ \text{W}$$

5. The standby power dissipation is $P_d = V_Q I_Q = V_{CC} I_Q = (15)(0.45) = 6.75\ W$.

6. The standby power dissipation found in (5) is the same as the average power supplied from the dc source, so

$$\eta = \frac{2.53\ \text{W}}{6.75\ \text{W}} = 0.375$$

4-5-2 Class-B Amplifier

Transistor operation is class B when output current varies during only one half-cycle of a sine-wave input. The transistor is in its active region only during a positive half-cycle or only during a negative half-cycle of the input , in practical amplifiers, two transistors are operated class B: one to amplify positive signal variations and the other to amplify negative signal variations. The output is the composite waveform obtained by combining by each .

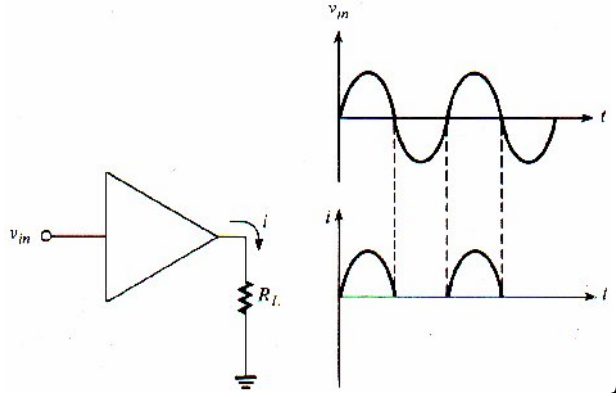


Figure 4-12 In class-B operation, output current variations occur during only each positive or each negative half-cycle of input.

4-5-2-1 Push-Pull -Amplifier Principles

A push-pull amplifier uses two output devices(typically two transistors) to drive a load, one device is responsible for driving current through the load in one direction(conducts only when the input is positive) (pushing), while the other device drives current through the load in the opposite direction(conducts only when the input is negative) (pulling).

In fig 4-13 the output amplifying device 1 drives current it through the load in one direction(base-to-emitter voltage is positive as in NPN transistors) while 2 is cut off, and device 2 drives current in the opposite direction while 1 is cut off. we must make provisions for load current to flow through a complete circuit, so when amplifying device 1 is cut off, it cannot conduct current produced by device 2, and vice versa.

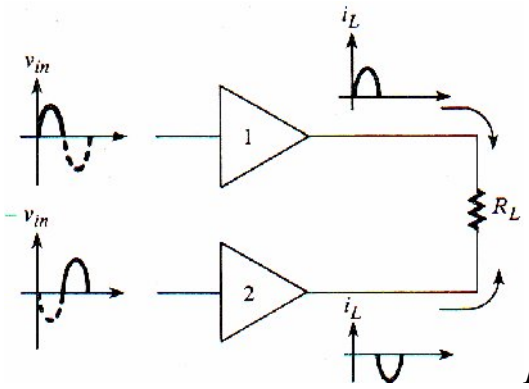


Figure 4-13 The principle of class-B, push-pull operation.

4-5-2-2 Push-Pull Amplifiers with Output Transformers

Fig 4-14 a center-tapped output transformer used in a push-pull amplifier arrangement that permits current to flow in both directions through a load even though one or the other of the amplifying devices is always cut off. the primary winding is connected between the transistor collectors and that its center tap is connected to the dc supply V_{CC} .

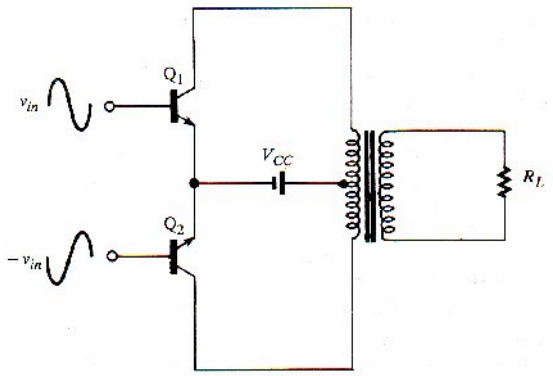
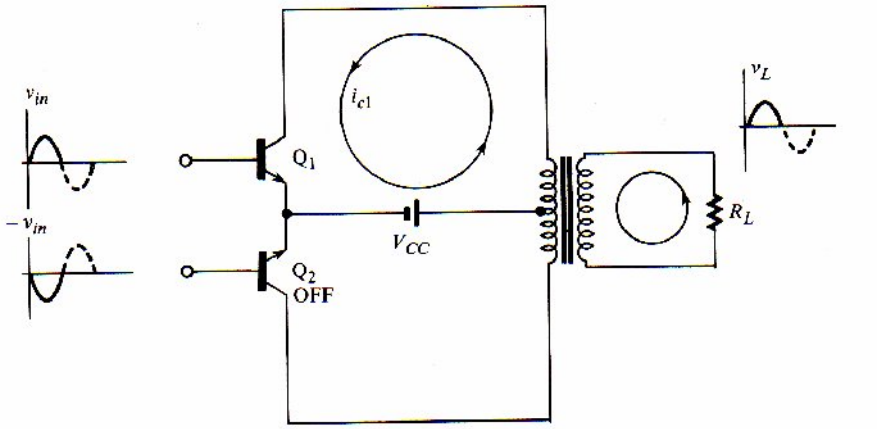


Figure 4-14 A center-tapped output transformer



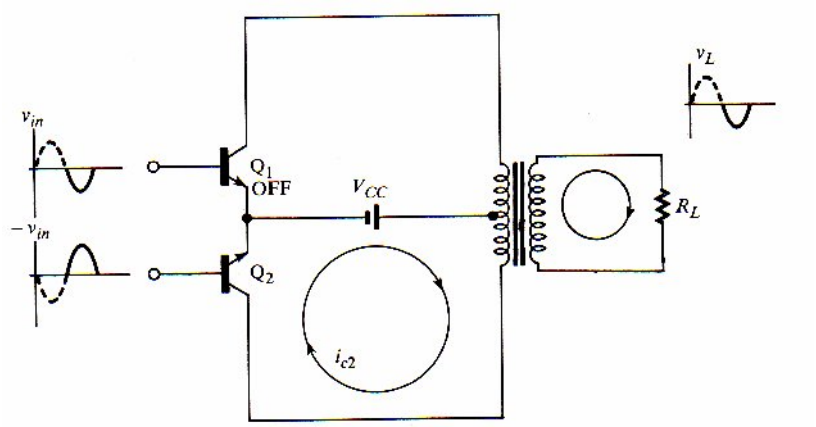
(a) When v_{in} is positive, Q_1 conducts and Q_2 is cut off. A counterclockwise current is induced in the load.

Figure 4-15(a)

In 4-15(a), the input to Q_1 is the positive half-cycle of the signal, and since the input to Q_2 is out-of-phase with that to Q_1, Q_2 is driven by a negative half-cycle.

the positive base voltage on Q_1 causes it to turn on and conduct current in the counterclockwise(assumed positive) path . The negative base voltage on Q_2 keeps that transistor cut off. In fig 4-15(b), the input signal on the base of Q_1 has gone negative, so its inverse on the base of Q_2 is positive. Therefore, Q_2 conducts current in the

clockwise(negative) path shown, and Q_1 is cut off. Current induced in the secondary winding is in the direction opposite.



(b) When v_{in} is negative, Q_2 conducts and Q_1 is cut off. A clockwise current is induced in the load.

Figure 4-15(b)

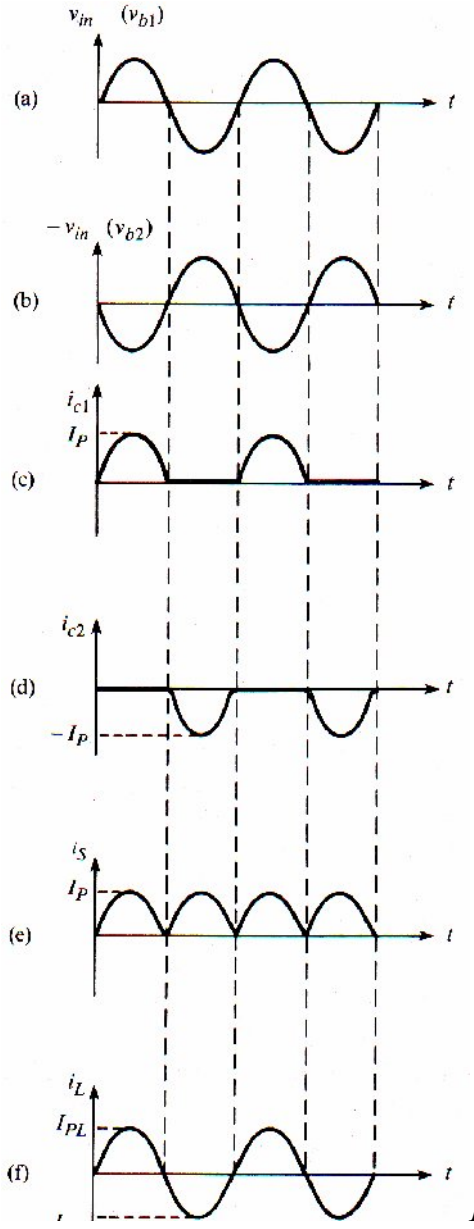


Figure 4-16 A timing diagram over two full cycles of input

Fig 4-16 the complete current waveforms are shown over two full cycles of input. Fig4-16(e) shows that the current is from the power supply varies from 0 to the peak value I_p every half-cycle

4-5-2-3 Class-B Efficiency

a class-B power amplifier is that it is possible to achieve an efficiency greater than that attainable in a class-A amplifier. The improvement in efficiency stems from the fact that no power is dissipated in a transistor during the time intervals that it is cut off. assuming ideal conditions: perfectly matched transistors and zero resistance in the transformer windings. The current supplied by each transistor is a half-wave-rectified waveform, Let I_p represent the peak value of each. Then the peak value of the current in the secondary winding, which is the same as the peak load current I_{PL} is:

$$I_{PL} = (N_p/N_s)I_P \text{ ----------4-42}$$

Similarly, the peak value of the load voltage is

$$V_{PL} = (N_s/N_p)V_P \text{ ---------4-43}$$

Vp is the peak value of the primary (collector) voltage. Since the load voltage and load current are sinusoidal, the average power delivered to the load is:

$$P_L = \frac{V_{PL}I_{PL}}{2} = \frac{(N_s/N_p)V_P(N_p/N_s)I_P}{2} = \frac{V_PI_P}{2} \text{ ----------4-44}$$

the power-supply current is a full-wave-rectified waveform having peak value I_p. The dc, or average, value of such a waveform is known to be $2I_p/\pi = 0.636I_P$. Therefore, the average power delivered to the circuit by the dc supply is:

$$P_S = \frac{2I_PV_{CC}}{\pi} \text{ ----------4-45}$$

The efficiency is then

$$\eta = \frac{P_L}{P_S} = \frac{V_PI_P/2}{2I_PV_{CC}/\pi} = \frac{\pi V_P}{4\,V_{CC}} \text{ ----------4-46}$$

Under maximum signal conditions, $V_p = V_{CC}$ and (4-46) becomes

$$\eta(\text{max}) = \frac{\pi}{4} = 0.785 \text{ ----------4-47}$$

Equ4-47 shows that a class-B push-pull amplifier can be operated with a much higher efficiency than the class-A amplifiers. Furthermore, unlike the case of class-A amplifiers, the power dissipated in the transistors is 0 under standby (zero signal) conditions, because both transistors are cut off. A general expression for the total power dissipated in the transistors can be obtained by realizing that it equals the difference between the total power supplied by the dc source and the total power delivered to the load:

$$P_d = \frac{2I_PV_{CC}}{\pi} - \frac{V_PI_P}{2} \text{ ----------4-48}$$

pd is maximum when $V_p=2Vcc/\pi=0.636Vcc$. the maximum pd does not occur when maximum load power is delivered ($V_p=V_{CC}$), but at the intermediate level $V_p = 0.636Vcc$.

Example 4-7: *The push-pull amplifier in fig4-14 has V_{CC} = 20V and R_L = 10Ω. The total number of turns on the primary winding is 100 and the secondary winding has 50 turns. Assume that the transformer has zero resistance.*

1. Find the maximum power that can be delivered to the load.

2. Find the power dissipated in each transistor when maximum power is delivered to the load.

3. Find the power delivered to the load and the power dissipated in each transistor when transistor power dissipation is maximum.

Solution. 1. *The turns ratio between each half of the primary and the secondary is Np/Ns = (100/2):50 = 50:50. Therefore, the peak values of primary and secondary voltages are equal, as are the peak values of primary and secondary current.*

$$V_P(\text{max}) = V_{PL}(\text{max}) = V_{CC} = 20\text{ V}$$
$$I_P(\text{max}) = I_{PL}(\text{max}) = V_{CC}/R_L = (20\text{ V})/(10\ \Omega) = 2\text{ A}$$

Therefore

$$P_L(\text{max}) = \frac{V_P(\text{max})I_P(\text{max})}{2} = \frac{(20)(2)}{2} = 20\text{ W}$$

2.

$$P_d = \frac{2I_PV_{CC}}{\pi} - \frac{V_PI_P}{2} = \frac{2(2)(20)}{\pi} - 20 = 5.46\text{ W}$$

Since 5.46 W is the total power dissipated by both transistors, each dissipates one-half that amount, or 2.73 W.

3. Transistor power dissipation is maximum when V_p = 0. 636V_{CC} = (0.636)(20) = 12.72V. Then

$$I_P = I_{PL} = \frac{12.72\text{ V}}{10\ \Omega} = 1.272\text{ A}$$

And

$$P_{t.} = \frac{V_PI_P}{2} = \frac{(12.72)(1.272)}{2} = 8.09\text{ W}$$
$$P_d(\text{max}) = \frac{2I_PV_{CC}}{\pi} - \frac{V_PI_P}{2} = \frac{2(1.272)(20)}{\pi} - 8.09 = 8.09\text{ W}$$

The maximum power dissipation in each transistor is then 8.09/2 = 4.05 W.

The preceding example demonstrates some results that are true for push-pull amplifiers:

1-When P_d is maximum, its value equals power delivered to the load

2-the maximum total P_d equals approximately 40% of the maximum power that can be delivered to the load.

4-5-2-4 Push-Pull Drivers

In fig4-17 a phase-splitter, used instead of a driver transformer to produce equal-amplitude, out-of-phase drive signals. The push-pull amplifier must be driven by out-of-phase input signals. in the secondary winding has a grounded center tap that effectively splits the secondary voltage into two out-of-phase signals, each having one-half the peak value of the total secondary voltage. Since the center point is at ground, the voltage from A to ground v_A must be (+3V) and from B to ground v_B must be (-3V):then $v_{AB} = v_A - v_B = 3 - (-3) = +6$ V . this called

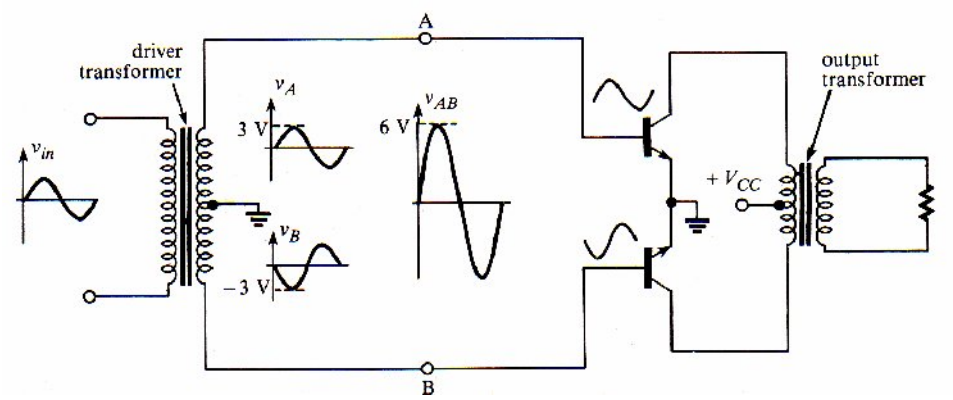
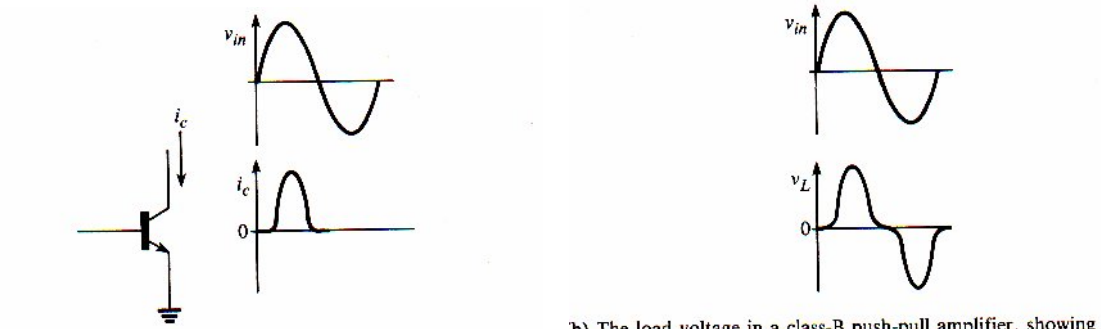


Figure 4-17 Using a driver transformer to create equal-amplitude, out-of-phase drive signals (v_A and v_B) for a push-pull amplifier

4-5-2-5 Distortion in Push-Pull Amplifiers

Crossover Distortion

A forward-biasing voltage applied across a PN junction must be raised to a certain level (about 0.7V for Si) before the junction will conduct any significant current. Similarly, the voltage across the base-emitter junction of a transistor must reach that level before any appreciable base current, and hence collector current, can flow. The drive signal applied to a class-B transistor must reach a certain minimum level before its ic is properly in the active region. This fact is the principal source of distortion in a class-B, push-pull amplifier, fig 4-18(a) shows that the initial rise of ic in a class-B transistor lags the initia1 rise of input voltage, for the reason we have described. Also, ic drops to 0 when the input voltage approaches 0. in fig 4-18(b) the voltage wave form that is produced in the load of a push-pull amplifier when the distortion generated during each half-cycle by each class-B transistor is combined.



(a) Collector current in a class-B transistor does not follow input voltage in the regions near 0 (crossovers)

(b) The load voltage in a class-B push-pull amplifier, showing the combined effects of the distortion generated during each half-cycle of input

Figure 4-18 Crossover distortion

This distortion is called crossover distortion, because it occurs where the composite waveform crosses the zero voltage axis. the effect of crossover distortion becomes more serious as the signal level becomes smaller.

4-5-3 Class-AB Operation

Crossover distortion can be reduced in a push-pull amplifier by biasing each transistor slightly into conduction. When a small forward-biasing voltage is applied across each base-emitter junction, and a small base current flows under no-signal conditions, it is not necessary for the base drive signal to overcome the built-in junction potential before active operation can occur. A simple voltage-divider bias network can be connected across each base for this purpose(fig 4-19) The base-emitter junctions are biased at about 0.7V for Si transistors so the collector current under no-signal conditions is about 1 % of its peak signal value.

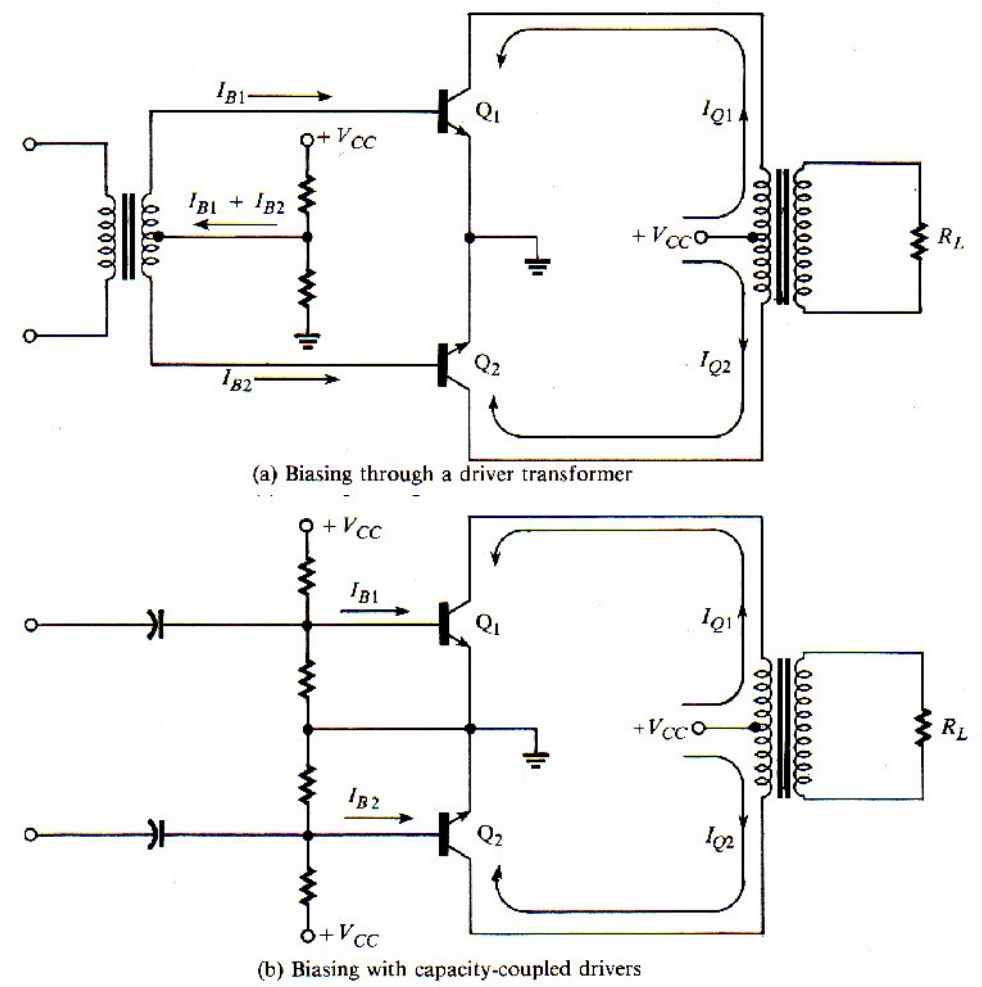


Figure 4-19 Methods for providing a slight forward bias for push-pull transistors to reduce crossover distortion

When a transistor is biased slightly into conduction, output current will flow during more than one-half cycle of a sine-wave input(fig4-20). conduction occurs for more than one-half but less than a full cycle of input. This operation, which is neither class A nor class B, is called class-AB operation.

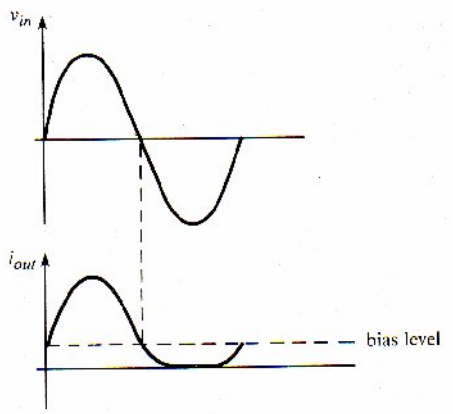


Figure 4-20 Class-AB operation. Output current i_{out} flows during more than one-half but less than a full cycle of input.

While class-AB operation reduces crossover distortion in a push-pull amplifier, it has the disadvantage of reducing amplifier efficiency. The fact that bias current is always present means that there is continuous power dissipation in both transistors, including the time intervals during which one of the transistors would be cut off if the operation were class B. The extent to which efficiency is reduced depends directly on how heavily the transistors are biased, and the maximum achievable efficiency is somewhere between that which can be obtained in class-A operation (0.25) and that attainable in class-B operation (0.785).

4-5-3-1 Transformer less Push-Pull Amplifiers
Complementary Push-Pull Amplifiers

The disadvantage of the push-pull amplifier circuits is the cost and bulk of their output transformers. High-power amplifiers in particular are encumbered by the need for very large transformers capable of conducting large currents without saturating. In fig4-21(a)a popular design using complementary (PNP and NPN) output transistors to eliminate the need for an output transformer in push-pull operation. This design also eliminates the need for a driver transformer or any other drive circuitry producing out-of-phase signals.

In fig4-21(b)the current flows in a counterclockwise path through the load when the input signal on the base of NPN transistor Q_1 is positive. The positive input simultaneously appears on the base of PNP transistor Q_2 and keeps it cut off. When the input is negative, Q_1 is cut off and Q_2 conducts current through the load in the opposite direction, as in fig4-21(c).

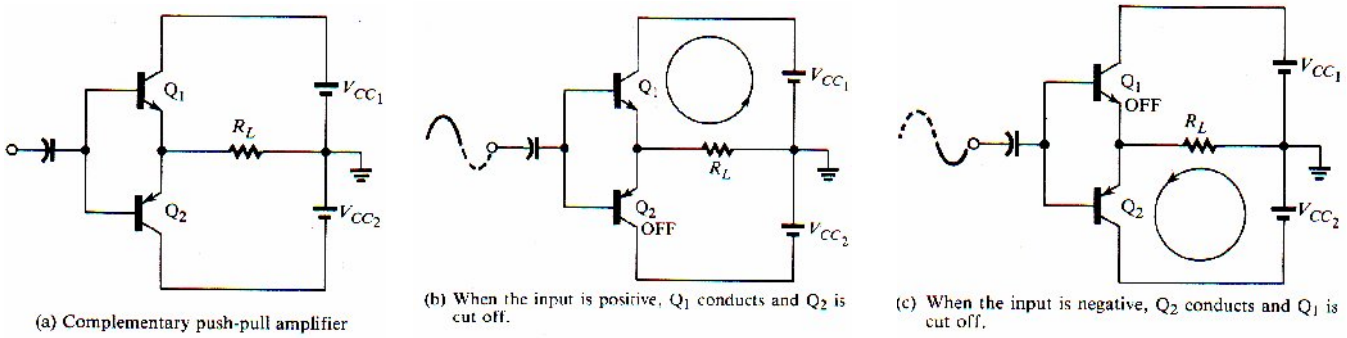


Figure 4-21 Push-pull amplification using complementary transistors. Note that the direction of current through RL alternates each half-cycle, as required.

each transistor in fig4-21 drives the load in an emitter-follower configuration. The advantageous consequence is that low-impedance loads can be driven from a low-impedance source. Also, the large negative feedback that is inherent in emitter follower operation reduces the problem of output distortion. The maximum positive voltage swing is V_{CC1} and the maximum negative swing is V_{CC2} . $|V_{CC1}| = |V_{CC2}| = V_{CC}$, so the maximum peak-to-peak swing is $2V_{CC}$ volts. Since the voltage gain is near unity, the input must also swing through $2V_{CC}$ volts to realize maximum output swing. Notice that under conditions of maximum swing, the cut-off transistor has a reverse-biasing collector-to-base voltage of $2V_{CC}$ volts.

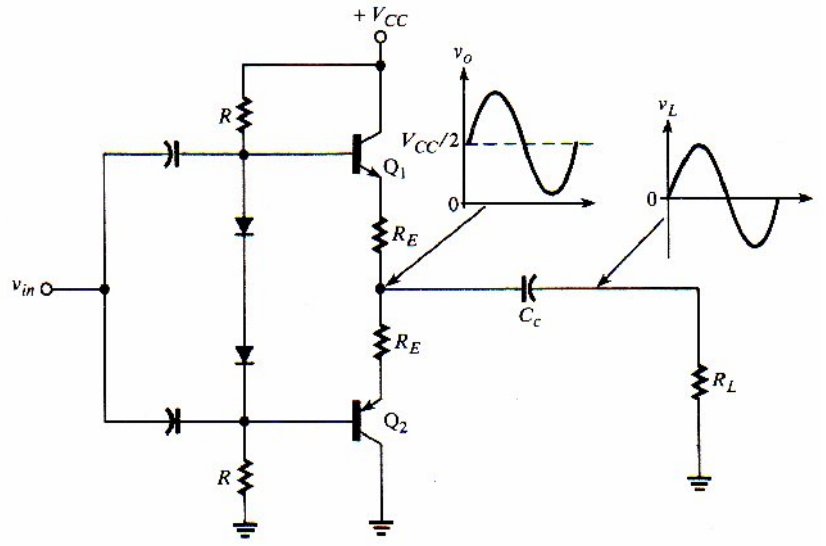
Example 4-8. *amplifier in fig 4-21 must deliver 30W to a15-Ω load under maximum drive.*
1. What is the minimum value required for each supply voltage?
2. What minimum collector-to-base breakdown-voltage rating should each transistor have?
Solution:1.

$$P_L(\max) = \frac{V_p^2(\max)}{2R_L}$$

$$V_p(\max) = \sqrt{2R_L P_L(\max)} = \sqrt{2(15)(30)} = 30 \text{ V}$$

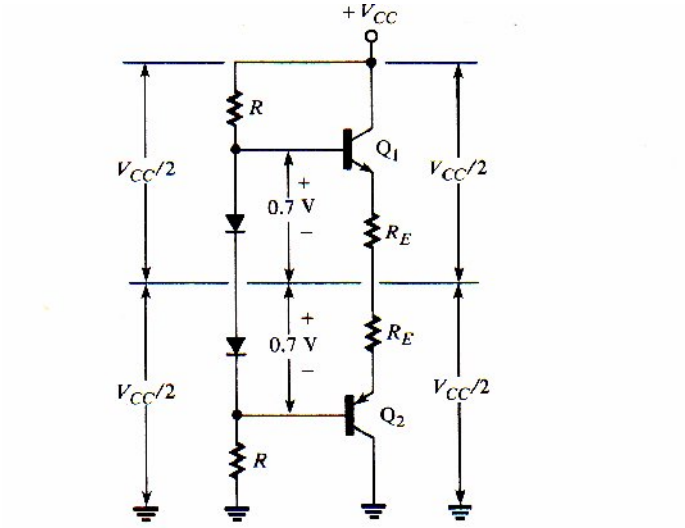
Therefore, for maximum swing $V_{CC} = V_{p(max)} = 30V$ i.e. $V_{CC1} = +30$ V & $V_{CC2} = -30V$.
2.The minimum rated breakdown is $2V_{CC} = 60$ V.

Fig4-22(a) shows the complementary amplifier that can be operated with a single power supply because the output V_O is biased at half the supply voltage and is capacitor-coupled to the load.
The resistor-diode network connected across the transistor bases is used to bias each transistor near the threshold of conduction. Crossover distortion can be eliminated by inserting another resistor (not shown in the figure) in series with the diodes to bias the transistors further into AB operation.



(a) The output is biased at $V_{CC}/2$ volts.

Assuming that all components are perfectly matched, the supply voltage will divide equally across each half of the amplifier, as fig4-22(b).



(b) DC bias voltages (All components are assumed to be perfectly matched.)

Figure 4-22 Complementary push-pull amplifier using a single power supply

Since each half of the amplifier has V_{CC} /2 volts across it, the forward-biased diode drops appear across the base-emitter junctions with the proper polarity to bias each transistor towards conduction.

In ac operation, when input v_1 is positive and Q_1 is conducting, current is drawn from the power supply and flows through Q_1 to the load. When Q_1 is cut off by a negative input. no current can flow from the supply. At those times, Q_2 is conducting and capacitor C_C discharges through that transistor. Thus, current flows from the load, through C_C and through Q_2 to ground whenever the input is negative. The R_L C_C time constant must be much greater than the period of the lowest signal frequency. The lower cutoff frequency is given by

$$f_1(C_c) = \frac{1}{2\pi(R_L + R_E)C_c} \text{ Hz} \quad \text{----------4-49}$$

The peak load current is the peak input voltage V_P divided by R_L+R_E

$$I_{PL} = \frac{V_P}{R_L + R_E} \quad \text{----------4-50}$$

Therefore, the average ac power delivered to the load is

$$P_L = \frac{I_{PL}^2 R_L}{2} = \frac{V_P^2 R_L}{2(R_L + R_E)^2} \quad \text{----------4-51}$$

Since current is drawn from the power supply only during positive half-cycles of input. the supply-current waveform is half-wave rectified, with peak value V_P /(R_L+R_E) Therefore, the average value of the supply current is

$$I_S(\text{avg}) = \frac{V_P}{\pi(R_L + R_E)} \quad \text{----------4-52}$$

and the average power from the supply is

$$P_S = V_{CC} I_S(\text{avg}) = \frac{V_{CC} V_P}{\pi(R_L + R_E)} \quad \text{----------4-53}$$

Dividing (4-51) by (4-53), we find the efficiency to

$$\eta = \frac{P_L}{P_S} = \frac{\pi}{2}\left(\frac{R_L}{R_L + R_E}\right)\left(\frac{V_P}{V_{CC}}\right) \text{----------4-54}$$

The efficiency is maximum when the peak voltage V_P has its maximum possible value, $V_{CC}/2$.

$$\eta(\max) = \frac{\pi}{2}\left(\frac{R_L}{R_L + R_E}\right)\left(\frac{V_{CC}/2}{V_{CC}}\right) = \frac{\pi}{4}\left(\frac{R_L}{R_L + R_E}\right) \text{----------4-55}$$

Eq4-54 & 4-55 shows that efficiency decreases, when R_E is increased. If R_E=0, then the maximum possible efficiency becomes ή(max)= π/4 = 0.785, the theoretical maximum for a class-B amplifier.

Example 4-9: *Assuming that all components in fig 4-23 are perfectly matched find*
1. the base-to-ground voltages V_{B1} and V_{B2} of each transistor,
2. the power delivered to the load under maximum signal conditions,
3. the efficiency under maximum signal conditions, and
4. the value of capacitor Cc if the amplifier is to be used at signal frequencies down to 20Hz.

Solution. *1. Since all components are matched, the supply voltage divides equally across the resistor-diode network, as shown in fig4-24, Then, as can be seen from the figure,*

$$V_{B1}=10+0.7 =10.7 \text{ V} \;\&\; V_{B2} = V_{B1} - 1.4 = 9.3 \text{ V}$$

2. with $V_{p(max)}$ = Vcc/2 = 10,

$$P_L(\max) = \frac{V_P^2(\max)R_L}{2(R_L + R_E)^2} = \frac{10^2(10)}{2(10 + 1)^2} = 4.132 \text{ W}$$

3.

$$\eta(\max) = \frac{\pi}{4}\left(\frac{R_L}{R_L + R_E}\right) = \frac{\pi}{4}\left(\frac{10}{11}\right) = 0.714$$

4.

$$C_c = \frac{1}{2\pi(R_L + R_E)f_1(C_c)} = \frac{1}{2\pi(11)(20)} = 723 \ \mu\text{F}$$

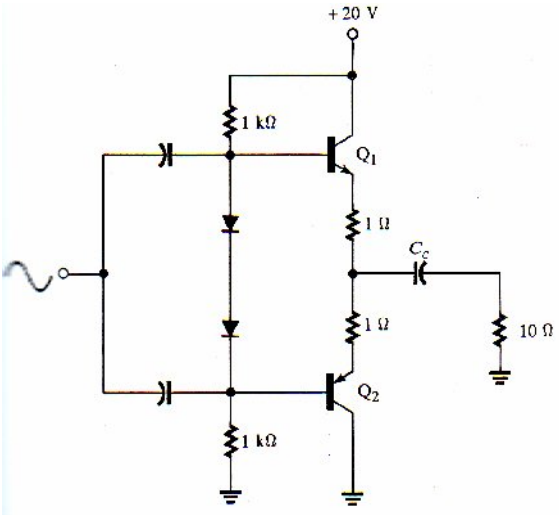


Figure 4-23 (Example 4-8)

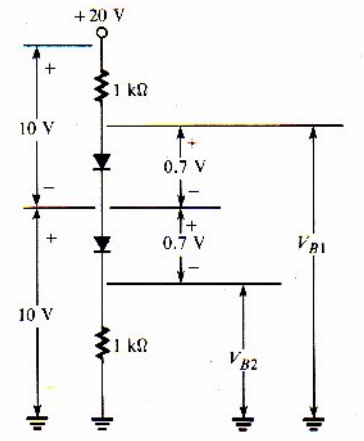


Figure 4-24 (Example 4-8)

This result demonstrates a principal disadvantage of the complementary, single-supply push-pull amplifier: the coupling capacitor must be quite large to drive a low-impedance load at a low frequency. These operating requirements are typical for audio power amplifiers.

Example 4-10. *Computing Maximum Power and Maximum Efficiency. use the parameters in Example 4-9 and comment on the results.*

Solution. *The power delivered to the load under maximum signal conditions is found by substituting* $V_p = Vcc/2$:

$$P_L(\max) = \frac{(V_{CC}/2)^2 R_L}{2(R_L + R_E)^2} = \frac{V_{CC}^2 R_L}{8(R_L + R_E)^2}$$

The efficiency under maximum signal conditions is:

$$\eta(\max) = \frac{\pi}{4}\left(\frac{R_L}{R_L + R_E}\right) = 0.7853981 R_L/(R_L + R_E)$$

4-5-4 Class-C Amplifiers

A class-C amplifier is one whose output conducts load current during less than one-half cycle of an input sine wave. Fig 4-25 is a typical class-C current waveform, show that the total angle during which current flows is less than 180˚. This angle is called the conduction angle , θ_C *. Of course, the output of a class-C amplifier is a highly distorted version of its input. It could not be used in an application requiring high fidelity, such as an audio amplifier. Class-C amplifiers are used primarily in high-power, high-frequency applications, such as radio-frequency transmitters. In these applications, the high-frequency pulses handled by the amplifier are not themselves the signal, but constitute what is called the carrier for the signal. The signal is transmitted by varying the amplitude of the carrier, using the process called amplitude modulation (AM). The signal is recovered in a receiver by filtering out the carrier frequency. The principal advantage of a class-C amplifier is that it has a very high efficiency.*

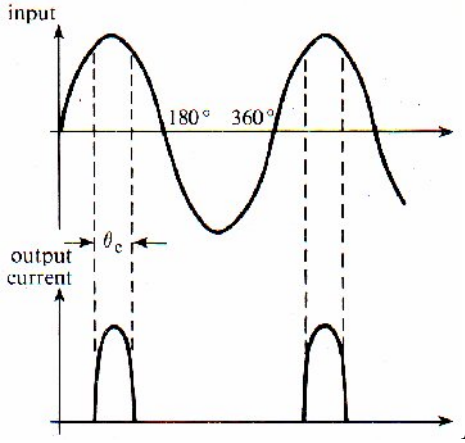


Figure 4-25 Output current in a class-C amplifier

Fig 4-26 shows a simple class-C amplifier with a resistive load, the base of the NPN transistor is biased by a negative voltage, $-V_{BB}$*, connected through a coil labeled RFC. The RFC is a radio-frequency choke whose inductance presents a high impedance to the high-frequency input and thereby prevents the dc source from shorting the ac input. In order for the transistor to begin conducting, the input must reach a level sufficient to overcome both the negative bias and the* V_{BE} *drop of about 0.7 V:*

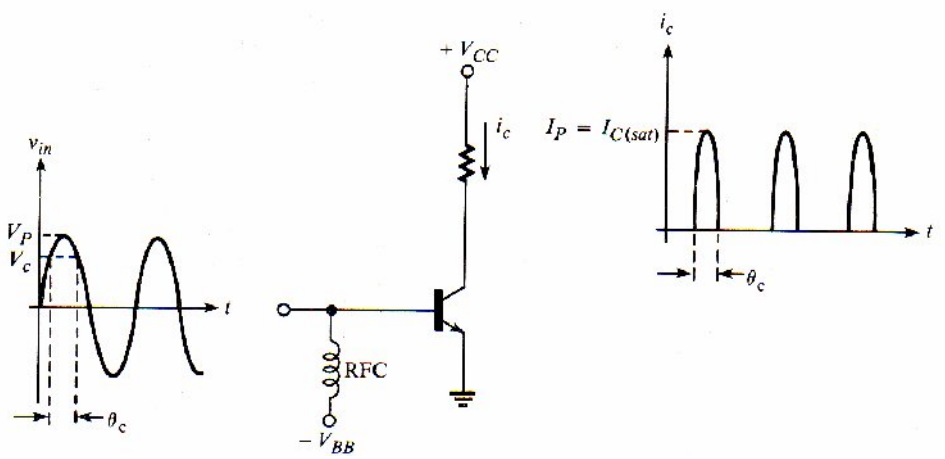


Fig 4-26 class-C amplifier with resistive load, the transistor conducts when $V_{in} \geq |V_{BB}| + 0.7$

$$V_c = |V_{BB}| + 0.7 \text{-----4-56}$$

V_C is the input voltage at which the transistor begins to conduct, the transistor is cut off until V_{in} reaches V_C, then it conducts, and then it cuts off again when V_{in} falls below V_C .The more negative the value of V_{BB}, the shorter the conduction interval. In most class-C applications, the amplifier is designed so that V_P is just sufficient to drive the transistor into saturation.
The conduction angle θ_C in Fig 4-25 can be found from

$$\theta_c = 2 \arccos\left(\frac{V_c}{V_P}\right) \text{---------4-57}$$

V_P drives the transistor to saturation. If V_P only just reaches V_C then θ_C=2 arcos(1) = 0°.
if V_{BB} = 0, then V_C = 0.7, (V_C / V_P) ≈ 0, and θ_C=2 arcos(0)=180°, which corresponds to class-B operation.
Fig 4-27 shows the class-C amplifier as it is normally operated, with an LC tank network in the collector circuit. Recall that the tank is a resonant network whose center frequency, assuming small coil resistance, is closely approximated by

$$f_o \approx \frac{1}{2\pi\sqrt{LC}} \text{----------4-58}$$

The purpose of the tank is to produce the fundamental component of the pulsed, class-C waveform, which has the same frequency as V_{in}. The configuration is called a tuned amplifier, and the center frequency of the tank is set equal to (tuned to) the input frequency. There are several ways to view its behavior as an aid in understanding how it recovers the fundamental frequency.
We may regard the tank as a highly selective (high Q) filter that suppresses the harmonics in the class-C waveform and passes its fundamental.
We may also recall that the voltage gain of the transistor equals the impedance in the collector circuit divided by the emitter resistance. Since the impedance of the tank is very large at its center frequency, the gain is correspondingly large at that frequency, while the impedance and the gain at harmonic frequencies are much smaller.

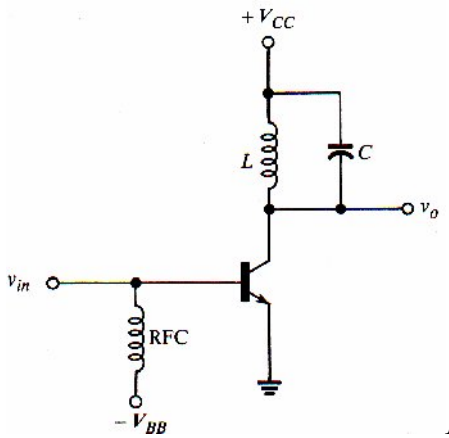


Fig4-27 A tuned class-C amp with an LC tank circuit as load

The amplitude of the fundamental component of a class-C waveform depends on the conduction angle θ_C . The greater the conduction angle, the greater the ratio of the amplitude of the fundamental component to the amplitude of the total waveform.
Let r_1 be the ratio of the peak value of the fundamental component to the peak value of the class-C waveform.

$$r_1 \approx (-3.54 + 4.1\theta_c - 0.0072\theta_c^2) \times 10^{-3} \text{----------4-59}$$

$0° \leq \theta_C \leq 180°$. The values of r_1 vary from 0 to 0.5 as θ_C varies from 0° to 180°.
Let r_o be the ratio of the dc value of the class-C waveform to its peak value. r_o can be found:

$$r_0 = \frac{\text{dc value}}{\text{peak value}} = \frac{\theta_c}{\pi(180)} \text{----------4-60}$$

$0° \leq \theta c \leq 180°$. The values of r_o vary from 0 to $1/\pi$ as θ_C varies from 0 to 180°.
The efficiency of a class-C amplifier is large because very little power is dissipated when the transistor is cut off, and it is cut off during most of every full cycle of input. the output power at the fundamental frequency under maximum drive conditions is

$$P_o = \frac{(r_1 I_P)V_{CC}}{2} \text{-------4-61}$$

I_p is the peak output (collector) current. The average power supplied by the dc source is V_{CC} times the average current drawn from the source. Since current flows only when the transistor is conducting, this current waveform is the same as the class-C collector-current waveform having peak value I_p. Therefore,

$$P_S = (r_0 I_P)V_{CC} \text{--------4-62}$$

The efficiency is then

$$\eta = \frac{P_o}{P_S} = \frac{r_1 I_P V_{CC}}{2 r_0 I_P V_{CC}} = \frac{r_1}{2 r_0} \text{-------4-62}$$

***Example 4-11**. A class-C amplifier has a base bias voltage of - 5V and V_{CC}=30V. it is determined that a peak input voltage of 9.8V at 1 MHz is required to drive the transistor to its saturation current of 1.8 A.*

1. Find the conduction angle.
2. Find the output power at 1 MHz.
3. Find the efficiency.
4. If an LC tank having C= 200 pF is connected in the collector circuit, find the inductance necessary to tune the amplifier.

Solution.*1.* $V_C = |V_{BB}| + 0.7 = 5 + 0.7 = 5.7\ V.$

$$\theta_c = 2\arccos\left(\frac{V_c}{V_P}\right) = 2\arccos\left(\frac{5.7}{9.8}\right) = 108.9°$$

2. $r_1 \approx [-3.54 + 4.1(108.9) - 0.0072(108.9)^2] \times 10^{-3} = 0.357.$

$$P_o = \frac{(r_1 I_P)V_{CC}}{2} = \frac{(0.357)(1.8)(30)}{2} = 9.64\ \text{W}$$

3.

$$r_0 = \frac{\theta_c}{\pi(180)} = \frac{108.9}{\pi(180)} = 0.193$$

$$\eta = \frac{r_1}{2r_0} = \frac{0.357}{2(0.193)} = 0.925 \quad (\text{or } 92.5\%)$$

This result demonstrates that a very high efficiency can be achieved in a class-C amplifier.

4.

$$L = \frac{1}{(2\pi f_o)^2 C} = \frac{1}{(2\pi \times 10^6)^2 (200 \times 10^{-12})} = 0.127\ \text{mH}$$

5- Oscillators

An oscillator is a device that generates a periodic, ac output signal without any form of input signal required with only the dc supply voltage as an input. The output voltage can be either sinusoidal or nonsinusoidal. Two major classifications of oscillators are feedback oscillators and relaxation oscillators; an oscillator is designed to have a feedback path with known characteristics, so that a predictable oscillation will occur at a predetermined frequency.

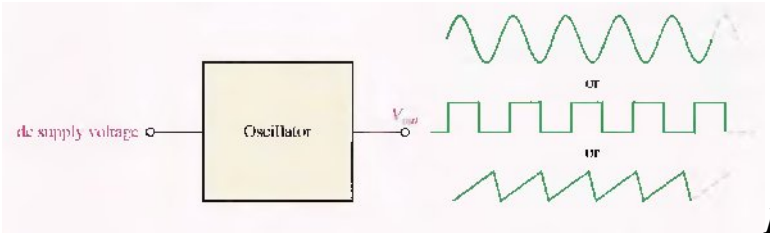


Fig 5-1The basic oscillator concept

5-1 Feedback Oscillators

One type of oscillator is the feedback oscillator, which returns a fraction of the output signal to the input with no net phase shift, resulting in a reinforcement of the output signal. After oscillations are started. The loop gain is maintained at 1 to maintain oscillations. A feedback oscillator consists of an amplifier for gain (either a discrete transistor or an op-amp) and a positive feedback circuit that produces phase shift and provides attenuation.

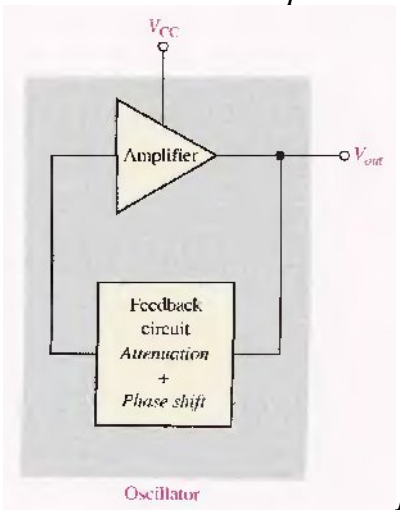


Fig2-5 Basic elements of a feedback oscillator.

5-2 Relaxation Oscillators

A second type is a relaxation oscillator uses an RC timing circuit to generate a waveform that is generally a square wave or other nonsinusoidal waveform, a relaxation oscillator uses a Schmitt trigger or other device that changes states to alternately charge and discharge a capacitor through a resistor.

5-3 Positive Feedback

Positive feedback is characterized by the condition wherein an in-phase portion of the output voltage of an amplifier is fed back to the input with no net phase shift. Resulting in a reinforcement of the output signal. The in-phase feedback voltage, V_f is amplified to produce

the output voltage, which in turn produces the feedback voltage. That is, a loop is created in which the signal sustains itself and a continuous sinusoidal output is produced. This phenomenon is called oscillation.

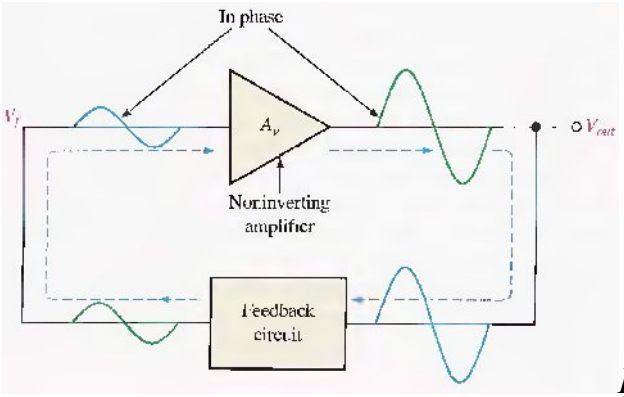


Fig 5-3 Positive feedback produces oscillation.

Two conditions are required for a sustained state of oscillation:

1. The phase shift around the feedback loop must be effectively 0.

2. The voltage gain, A_d, around the closed feedback loop (loop gain) must equal 1 (unity).

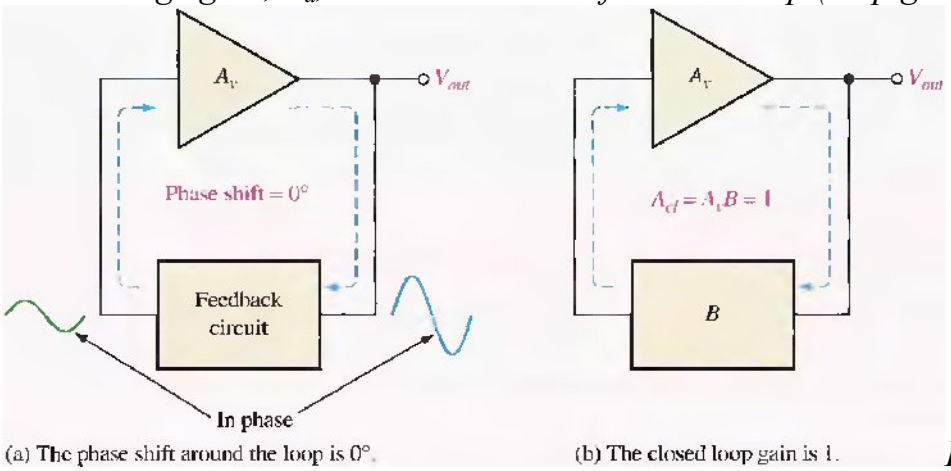


Fig 5-4General conditions

5-4 Start-Up Conditions

the unity-gain condition must be met for oscillation to be sustained. For oscillation to begin, the voltage gain around the positive feedback loop must be greater than 1 so that the amplitude of the output can build up to a desired level. The gain must then decrease to 1 so that the output stays at the desired level and oscillation is sustained. A question that normally arises is this: If the oscillator is initially off and there is no output voltage. How does a feedback signal originate to start the positive feedback buildup process? Initially a small positive feedback voltage develops from thermally produced broad-band noise in the resistors or other components or from power supply turn-on transients. The feedback circuit permits only a voltage with a frequency equal to the selected oscillation frequency to appear in phase on the amplifier's input. This initial feedback voltage is amplified and continually reinforced, resulting in a buildup of the output voltage as discussed.

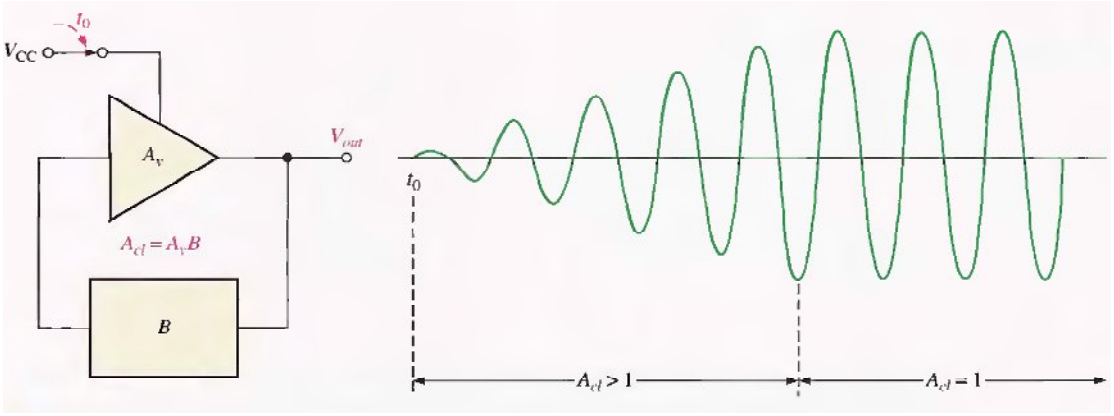


Fig5-5 When oscillation starts at to, the condition $A_d > 1$ causes the sinusoidal output voltage amplitude to build up to a desired level. Then A_d decreases to 1 and maintains the desired amplitude.

5-5 The Barkhausen Criterion

What we mean by "feedback" feedback to where? In reality, it makes no difference where, because we have a closed loop with no summing junction at which any external input is added. Thus, we could start anywhere in the loop and call that point both the "input" and the "output"; we could think of the "feedback" path as the entire path through which signal flows in going completely around the loop. Amplifier having gain A and a feedback path having gain β. Every oscillator must have an amplifier, or equivalent device, in order for the system oscillate, the loop gain Aβ must satisfy the barkhausen criterion, namely,

$$A\beta = 1 \text{ ----------5-1}$$

The unity loop-gain criterion for oscillation is often called positive feedback.
To understand and apply the Barkhausen criterion, we must regard both the gain and the phase shift of Aβ as functions of frequency. To show the dependence of the loop gain Aβ on frequency, we write Aβ(jw), a complex phasor that can be expressed in both polar and rectangular form:

$$A\beta(j\omega) = |A\beta|\angle\theta = |A\beta|\cos\theta + j|A\beta|\sin\theta \text{ ----------5-2}$$

$|A\beta|$ is the gain magnitude, a function of frequency, and θ is the phase shift, also a function of frequency. The Barkhausen criterion requires that

$$|A\beta| = 1 \text{ ----------5-3}$$

$$\theta = \pm 360°n \text{ ----------5-4}$$

n is any integer, including 0. In polar and rectangular forms, the Barkhausen criterion is expressed as

$$A\beta(j\omega) = 1\angle\pm 360°n = 1 + j0 \text{ ----------5-5}$$

Example5-1:*The gain of a certain amplifier as a function of frequency is $A(jw)=-16 \times 10^6/jw$. A feedback path connected around it has $\beta(jw)=10^3/(2 \times 10^3 + jw)^2$. Will the system oscillate? If so, at what frequency?*

Solution: *The loop gain is*

$$A\beta = \left(\frac{-16 \times 10^6}{j\omega}\right)\left[\frac{10^3}{(2 \times 10^3 + j\omega)^2}\right] = \frac{-16 \times 10^9}{j\omega(2 \times 10^3 + j\omega)^2}$$

To determine if the system will oscillate, we will first determine the frequency, at which the phase angle of Aβ(θ)= 0 or a multiple of 360°. Using phasor algebra, we have

$$\theta = \underline{/A\beta} = \underline{/\frac{-16 \times 10^9}{j\omega(2 \times 10^3 + j\omega)^2}} = \underline{/-16 \times 10^9} + \underline{/1/j\omega} + \underline{/\frac{1}{(2 \times 10^3 + j\omega)^2}}$$

$$= -180° - 90° - 2\arctan(\omega/2 \times 10^3)$$

$$= -360° \quad \text{if } 2\arctan(w/2 \times 10^3) = 90°$$

Or

$$\arctan(\omega/2 \times 10^3) = 45°$$

$$\omega/2 \times 10^3 = 1$$

$$\omega = 2 \times 10^3 \text{ rad/s}$$

Thus, the phase shift around the loop is -360° at w = 2000 rad/s.
We must now check to see if the gain magnitude $|A\beta| = 1$ at $w = 2 \times 10^3$.
The gain magnitude is

$$|A\beta| = \left|\frac{-16 \times 10^9}{j\omega(2 \times 10^3 + j\omega)^2}\right| = \frac{|-16 \times 10^9|}{|j\omega|\,|(2 \times 10^3 + j\omega)|^2}$$

$$= \frac{16 \times 10^9}{\omega[(2 \times 10^3)^2 + \omega^2]}$$

Substituting $\omega = 2 \times 10^3$, we find

$$|A\beta| = \frac{16 \times 10^9}{2 \times 10^3(4 \times 10^6 + 4 \times 10^6)} = 1$$

Thus, the Barkhausen criterion is satisfied at $w = 2 \times 10^3$ rad/s and oscillation occurs at that frequency ($2 \times 10^3/2\pi = 318.3$ Hz).

Example 5-2: *illustrated an application of the polar form of the Barkhausen criterion, since we solved for/Aβ and then determined the frequency at which that angle equals -360°.*
It is instructive to demonstrate how the same result can be obtained using the rectangular form of the criterion: Aβ = 1 + j0. Towards that end, we first expand the denominator:

$$A\beta = \frac{-16 \times 10^9}{j\omega(2 \times 10^3 + j\omega)^2} = \frac{-16 \times 10^9}{j\omega(4 \times 10^6 + j4 \times 10^3\omega - \omega^2)}$$

$$= \frac{-16 \times 10^9}{j\omega[(4 \times 10^6 - \omega^2) + j4 \times 10^3\omega]} = \frac{16 \times 10^9}{4 \times 10^3\omega^2 - j\omega(4 \times 10^6 - \omega^2)}$$

To satisfy the Barkhausen criterion, this expression for Aβ must equal 1. We therefore set it equal to 1 and simplify:

$$1 = \frac{16 \times 10^9}{4 \times 10^3\omega^2 - j\omega(4 \times 10^6 - \omega^2)}$$

$$4 \times 10^3\omega^2 - j\omega(4 \times 10^6 - \omega^2) = 16 \times 10^9$$

$$(4 \times 10^3\omega^2 - 16 \times 10^9) - j\omega(4 \times 10^6 - \omega^2) = 0$$

In order for this expression to equal 0, both the real and imaginary parts must equal 0. Setting either part equal to 0 and solving for w will give us the same result we obtained before:

$$4 \times 10^3\omega^2 - 16 \times 10^9 = 0 \Rightarrow \omega = 2 \times 10^3$$
$$4 \times 10^6 - \omega^2 = 0 \Rightarrow \omega = 2 \times 10^3$$

5-6 The RC Phase-shift Oscillator

The simplest kinds of oscillators incorporating an operational amplifier can be constructed as in Fig 5-6. The amplifier is connected in an inverting configuration and drives three cascaded (high-pass) RC sections. The arrangement is called an RC phase-shift oscillator.

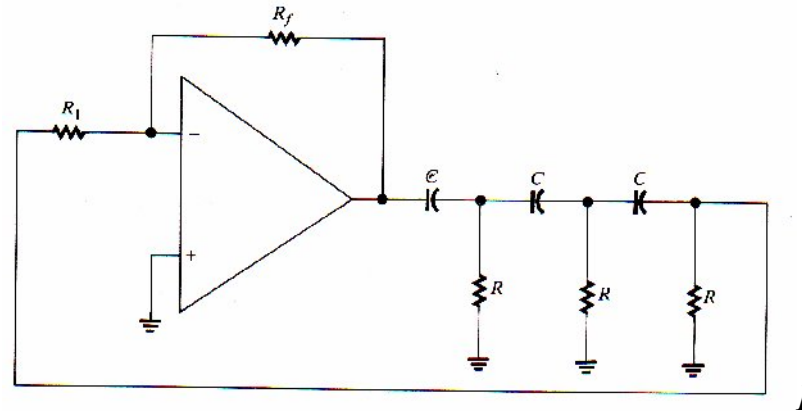


Fig5-6 An RC oscillator

The inverting amplifier causes a 180° phase shift in the signal passing through it, and the purpose of the cascaded RC sections is to introduce an additional 180° at some frequency. the output single of high-pass RC network leads its input by a phase angle that depends on the signal frequency.

When the signal passes through all three RC sections, there will be some frequency at which the cumulative phase shift is 180°. When the signal having that frequency is fed back to the inverting amplifier, the total phase shift around the loop will equal 180° + 180° = 360° (or, equivalently, - 180° + 180° = 0°) and oscillation will occur at that frequency, provided the loop gain is 1. The gain necessary to overcome the loss in the RC cascade and bring the loop gain up to 1 is supplied by the amplifier ($vo/vi = -R_f/R_1$). With considerable algebraic effort, that the feedback ratio determined by the RC cascade is

$$\beta = \frac{R^3}{(R^3 - 5RX_C^2) + j(X_C^3 - 6R^2X_C)} \text{----------5-6}$$

In order for oscillation to occur, the cascade must shift the phase of the signal by 180°, which means the angle of β must be 180°. When the angle of β is 180°, β is a purely real number. In that case, the imaginary part of the denominator of equation 5-6 is 0.

Therefore, we can find the oscillation frequency by finding the value of w that makes the imaginary part equal 0. Setting it equal to 0 and solving for w, we find

$$X_C^3 - 6R^2X_C = 0$$
$$X_C^3 = 6R^2X_C$$
$$X_C^2 = 6R^2$$
$$\frac{1}{(\omega C)^2} = 6R^2$$

$$\omega = \frac{1}{\sqrt{6}RC} \text{ rad/s} \qquad \text{----------5-7}$$

Or

$$f = \frac{1}{2\pi\sqrt{6}RC} \text{ Hz} \qquad \text{----------5-8}$$

R_1 in Fig 5-2 is effectively in parallel with the rightmost resistor R in the RC cascade, because the inverting input of the amplifier is at virtual ground. Therefore, when the feedback loop is closed by connecting the cascade to R_1, the frequency satisfying the phase criterion will be somewhat different than that predicted by equation 5-8.
If $R_1 >> R$, so that $R_1 \| R \approx R$, then equation 5-8 will closely predict the oscillation frequency.
We can find the gain that the amplifier must supply by finding the reduction in gain caused by the RC cascade by evaluating the magnitude of β at the oscillation frequency: $w = 1/(\sqrt{6}RC)$. At that frequency, the imaginary term in equation 5-6 is 0 and β is the real number

$$|\beta| = \frac{R^3}{R^3 - 5RX_C^2} = \frac{R^3}{R^3 - 5R\left(\frac{\sqrt{6}RC}{C}\right)^2}$$
$$= \frac{R^3}{R^3 - 30R^3}$$
$$= -1/29 \qquad \text{----------5-9}$$

The minus sign confirms that the cascade inverts the feedback at the oscillation frequency. We see that the amplifier must supply a gain of -29 to make the loop gain $A\beta = 1$. Thus:

$$R_f/R_1 = 29 \qquad \text{----------5-10}$$

Example 5-3: *Design an RC phase-shift oscillator that will oscillate at 100 Hz.*
Solution: *From equation 5-8,*

$$f = 100 = \frac{1}{2\pi\sqrt{6}RC}$$

Let C = 0.5μF. Then

$$R = \frac{1}{100(2\pi)\sqrt{6}(0.5 \times 10^{-6})} = 1300\ \Omega$$

To prevent R_1 from loading this value of R, we choose R_1=20 kΩ.
so that $R \| R_1 = 1300\Omega$
$R_f = 29\ R_1 = 29(20\ k\Omega) = 580\ k\Omega.$
R_f is made adjustable so the loop gain can be set precisely to 1

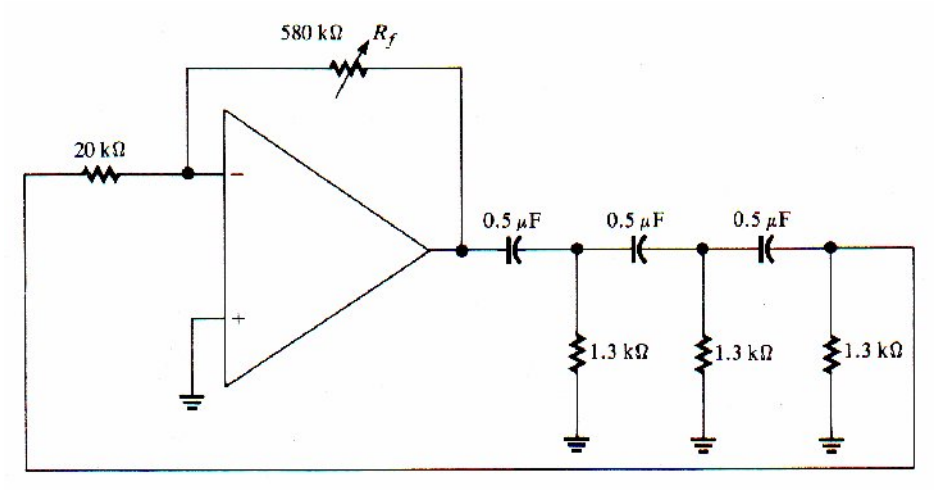


Figure 5-7 Ex 5-3

5-8 The Wien-bridge Oscillator

a widely used type of oscillator called a Wien bridge. The operational amplifier is used in a noninverting configuration, and the impedance blocks labeled Z_1 & Z_2 form a voltage divider that determines the feedback ratio.

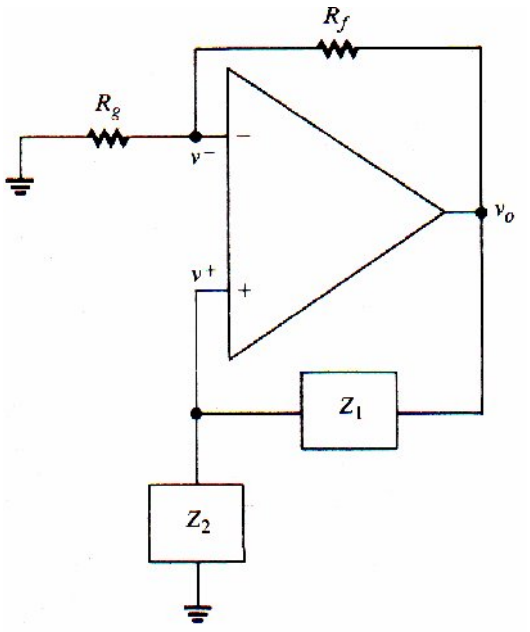


Fig 5-8 The Wien-bridge oscillator, Z_1& Z_2 determine the feedback ratio to the noninverting input, R_f & R_g control the magnitude of the loop gain

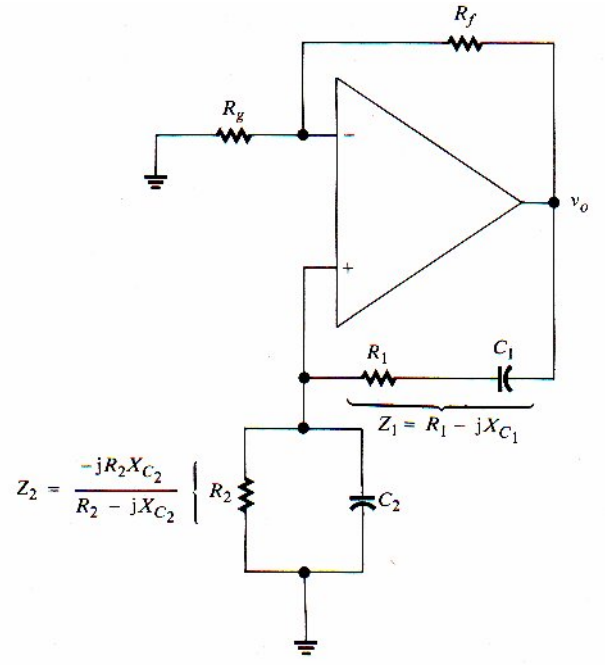


Fig 5-9 The Wien-bridge oscillator showing the RC networks that form: Z_1& Z_2 Therefore, the Amp must provide a gain of 3 to make the magnitude of the loop gain unity and sustain oscillation

Note that a portion of the output voltage is fed back through this impedance divider to the + input of the amplifier Resistors R_g & R_f determine the amplifier gain and are selected to make the magnitude of the loop gain equal to 1. If the feedback impedances are chosen properly, there will be some frequency at which there is zero phase shift in the signal fed back to the amplifier input (v^+). Since the amplifier is noninverting, it also contributes zero phase shift,

so the total phase shift around the loops is 0 at that frequency, as required for oscillation. In the most common version of the Wien-bridge oscillator, Z_1 is a series RC combination and Z_2 is a parallel RC combination

$$Z_1 = R_1 - jX_{C_1}$$

$$Z_2 = R_2 \parallel X_{C_2} = \frac{-jR_2X_{C_2}}{R_2 - jX_{C_2}}$$

$$\beta = \frac{v_o}{v^+} = \frac{Z_2}{Z_1 + Z_2} = \frac{-jR_2X_{C_2}/(R_2 - jX_{C_2})}{R_1 - jX_{C_1} - jR_2X_{C_2}/(R_2 - jX_{C_2})} \quad \text{----------5-11}$$

$$\frac{v_o}{v^+} = \frac{R_2X_{C_2}}{(R_1X_{C_2} + R_2X_{C_1} + R_2X_{C_2}) + j(R_1R_2 - X_{C_1}X_{C_2})} \quad \text{----------5-12}$$

In order for v+ to have the same phase as vo, this ratio must be a purely real number. Therefore, the imaginary term in (5-12 must be 0). Setting the imaginary term equal to 0 and solving for w gives us the oscillation frequency:

$$R_1R_2 - X_{C_1}X_{C_2} = 0$$

$$R_1R_2 = \left(\frac{1}{\omega C_1}\right)\left(\frac{1}{\omega C_2}\right)$$

$$\omega^2 = \frac{1}{R_1R_2C_1C_2}$$

$$\omega = \frac{1}{\sqrt{R_1R_2C_1C_2}} \text{ rad/s} \quad \text{----------5-13}$$

In most applications, the resistors are made equal and so are the capacitors: $R_1 = R_2 = R$ & $C_1 = C_2 = C$. In this case, the oscillation frequency becomes

$$\omega = \frac{1}{\sqrt{R^2C^2}} = \frac{1}{RC} \text{ rad/s} \quad \text{----------5-14}$$

$$f = \frac{1}{2\pi RC} \text{ Hz} \quad \text{----------5-15}$$

When: $R_1 = R_2 = R$ & $C_1 = C_2 = C$, the capacitive reactance of each capacitor at the oscillation frequency is:

$$X_{C_1} = X_{C_2} = \frac{1}{\omega C} = \frac{1}{\left(\frac{1}{RC}\right)C} = R$$

Substituting: $X_{c1} = X_{c2} = R = R_1 = R_2$ in equation 5-12, we find that the feedback ratio at the oscillation frequency is

$$\frac{v_o}{v^+} = \frac{R^2}{3R^2 + j0} = \frac{1}{3}$$

Since the amplifier gain is $(R_g + R_f) / R_g$, we require

$$\frac{R_g + R_f}{R_g} = 3, \text{ or } \quad 1 + \frac{R_f}{R_g} = 3 \Rightarrow \frac{R_f}{R_g} = 2 \quad \text{----------5-16}$$

Example 5-6: *Design a Wien bridge-oscillator that oscillates at 25 kHz.*

Solutions: *Let $C_1 = C_2 = 0.001\mu F$. Then, from equation 5-15,*

$$f = 25 \times 10^3 = \frac{1}{2\pi R(10^{-9})}$$

$$R = \frac{1}{2\pi(25 \times 10^3)(10^{-9})} = 6366\ \Omega$$

Let $R_g = 10\ k\Omega$. Then, from equation 5-16,

$$\frac{R_f}{R_g} = 2 \Rightarrow R_f = 20\ k\Omega$$

5-9 LC and crystal oscillator

Although the RC feedback oscillators, particularly the Wien bridge, are generally suitable for frequencies up to about I MHz, LC feedback elements are normally used in oscillators that require higher frequencies of oscillation.

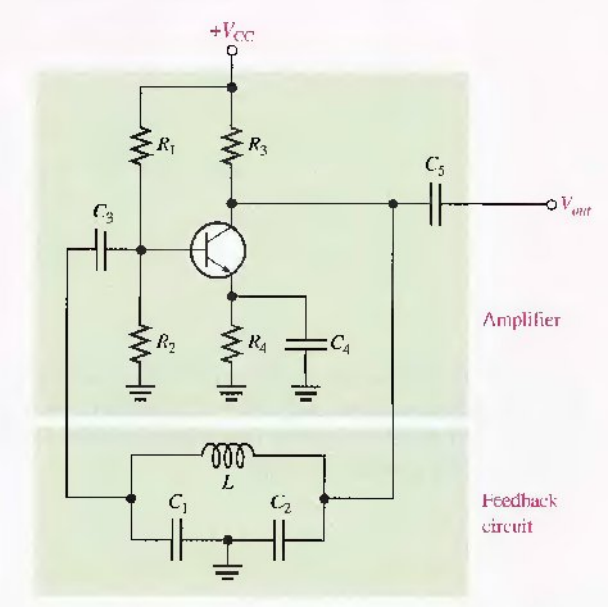


Fig5-10 A Colpitts with BJT as a gain element.

Also, because of the frequency limitation (lower unity-gain frequency) of most op-amps, discrete transistors (BJT or FET) are often used as the gain element in LC oscillators. One basic type of resonant circuit feedback oscillator is the Colpitts . As shown in Fig5-10 this type of oscillator uses an LC circuit in the feedback loop to provide the necessary phase shift and to act as a resonant filter that passes only the desired frequency of oscillation.

The approximate frequency of oscillation is the resonant frequency of the LC circuit and is established by the values of $C_1 > C_2$, and L according to this familiar formula:

$$f_r \cong \frac{1}{2\pi\sqrt{LC_T}} \text{ ----------5-17}$$

where C_T is the total capacitance. Because the capacitors effectively appear in series around the tank circuit, the total capacitance (C_T) is

$$C_T = \frac{C_1 C_2}{C_1 + C_2} \text{ ----------5-18}$$

Conditions for Oscillation and Start-Up

The attenuation, β , of the resonant feedback circuit in the Colpitts oscillator is basically determined by the values of C_1 & C_2 .
Fig5-11 shows that the circulating tank current is through both C_1 & C_2 (they are effectively in series). The voltage developed across C_2 is the oscillator's output voltage (V_{out}) and the voltage developed across C_1 is the feedback voltage (V_f), as indicated. The expression for the attenuation (β) is

$$B = \frac{V_f}{V_{out}} \cong \frac{IX_{C1}}{IX_{C2}} = \frac{X_{C1}}{X_{C2}} = \frac{1/(2\pi f_r C_1)}{1/(2\pi f_r C_2)} \text{----------5-19}$$

Canceling the 2πfr terms gives

$$B = \frac{C_2}{C_1} \text{----------5-20}$$

As you know, a condition for oscillation is $A_v \beta = 1$. Since $\beta = C_2 / C_1$,

$$A_v = \frac{C_1}{C_2} \text{----------5-21}$$

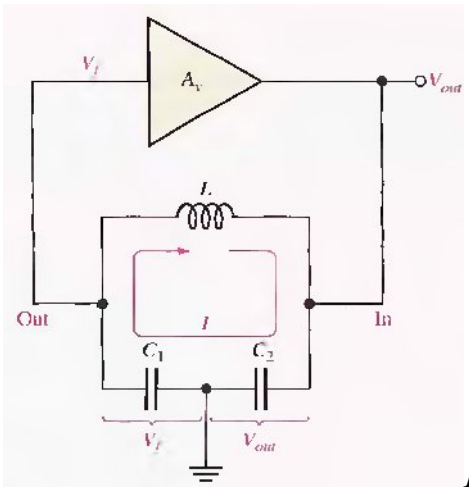


Fig 5-11The attenuation of the tank circuit is the output of the tank (V_f) divided by the input to the tank (V_{out}). $\beta = V_f / V_{out} = C_2 / C_1$. For $A_v \beta > 1$, A_v must be greater than C_1/C_2

A_v is the voltage gain of the amplifier. Which is represented by the triangle in Fig5-11 With this condition met, $A_v\beta = (C_1/C_2)(C_2/C_1) = 1$. Actually. For the oscillator to be self starting, $A_v\beta$ must be greater than 1 (that is, $A_v\beta > 1$). Therefore, the voltage gain must be made slightly greater than C_1/C_2.

$$A_v > \frac{C_1}{C_2} \text{----------5-22}$$

Loading of the Feedback Circuit Affects the Frequency of Oscillation

As indicated in Fig5-12. The input impedance of the amplifier acts as a load on the resonant feedback circuit and reduces the Q (resonant frequency = Q = f_o /BW typical value must be <=10) of the circuit. Recall from your study of resonance that the resonant frequency of a parallel resonant circuit depends on the Q, according to the following formula:

$$f_r = \frac{1}{2\pi\sqrt{LC_T}}\sqrt{\frac{Q^2}{Q^2+1}} \text{----------5-23}$$

for a Q greater than 10, the frequency is approximately $1/(2\pi\sqrt{LC_T})$.

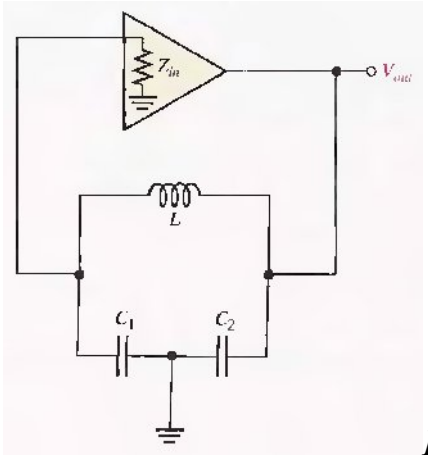
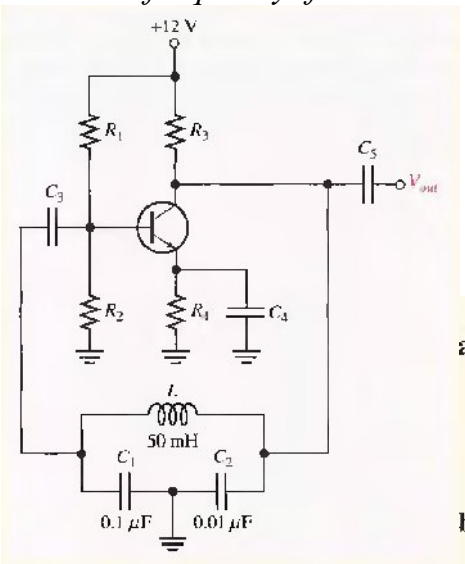


Fig5-12 Z_{in} loads the feedback circuit and lowers its Q,

Example5-4

(a) Determine the frequency for the oscillator in Fig5-13. Assume there is negligible loading on the feedback circuit and that its Q is greater than 10.

(b) Find the frequency if the oscillator is loaded to a point where the Q drops to 8.



a) $C_T = \dfrac{C_1 C_2}{C_1 + C_2} = \dfrac{(0.1\ \mu\text{F})(0.01\ \mu\text{F})}{0.11\ \mu\text{F}} = 0.0091\ \mu\text{F}$

$$f_r \cong \frac{1}{2\pi\sqrt{LC_T}} = \frac{1}{2\pi\sqrt{(50\ \text{mH})(0.0091\ \mu\text{F})}} = \mathbf{7.46\ kHz}$$

b) $f_r = \dfrac{1}{2\pi\sqrt{LC_T}}\sqrt{\dfrac{Q^2}{Q^2+1}} = (7.46\ \text{kHz})(0.9923) = \mathbf{7.40\ kHz}$