Synchronization

-In almost every receiver or demodulator performance, some level of signal synchronization is used. For example in the case of coherent phase demodulation (PSK), the receiver is assumed to be able to generate reference signals whose phases are identical (except perhaps for a constant offset) to those of the signaling alphabet at the transmitter.

-Digital communication systems using coherent modulation require three levels of synchronization
1-Phase, 2-Symbol, 3-Frame.

-Digital communication systems using noncoherent modulation require two levels of synchronization
1-Symbol, 2-Frame.

Since the modulation is not coherent, accurate phase lock is not required. Instead, noncoherent require frequency synchronization. Frequency synchronization differs from phase synchronization in that the replica of the carrier that is generated by the receiver is allowed to have arbitrary constant phase offset from the received carrier. Receiver designs can be simplified by removing the requirement to determine the exact value of the incoming carrier phase.

The receiver, in digital communication systems, has accurate knowledge about incoming symbol started and when it is over. This knowledge is required in order to know the proper symbol
integration interval (the interval over which energy is integrated prior to making symbol decision).

-It can be seen that symbol synchronization and phase synchronization are similar in that both involve producing in the receiver a replica of a portion of the transmitted signal.

-For phase synchronization, it is an accurate replica of the carrier.

-For symbol synchronization, it is a square wave at the symbol transition rate (the receiver must be able to produce a square wave for each incoming signals transitions between symbols). A receiver that is able to do this can be said to have symbol synchronization, or to be in symbol lock.

-In many communication systems an even higher level of synchronization is required. This is usually called frame synchronization. Frame synchronization is required when the information is organized in blocks, or messages of some uniform number of symbols (this occur, for example, if a block code is used for forward error control, or if the communication channel is used for several user as in TDMA). In the case of block coding, the decoder needs to know the boundaries between code words in order to decode the message correctly. In the case TDMA, it is necessary to know where the location of boundaries between channel users are, in order to route the information correctly.

-Similar to symbol synchronization, frame synchronization is equivalent to being able to generate a square wave at the frame rate,
with the zero crossing coincident with the transitions from one frame to the next.

-All of the discussion thus far had been oriented toward the receiving end of a communication link. There are many cases, when the transmitter assumes the more active role in synchronization by varying the time and frequency of its transmissions to receiver, as in the case of satellite communication network. In most of these cases, the transmitter knows on a return path from the receiver to determine the accuracy of its synchronization (two way communications are used in the transmitter synchronization). The transmitter synchronization is often called network synchronization.

**Synchronization costs and benefits**

1-The most obvious costs is in the need for additional hardware or software in the receiver for acquisition and tracking.

2-Extra time is required to achieve synchronization before commencing communications.

3-Error control coding is used.

**Frequency and phase synchronization**

- The heart of all synchronization circuits is the phase locked loop (PLL). A schematic diagram of the basic PLL is shown in fig(13.1). PLL is a servo control loop, whose controlled parameter is the phase of a locally generated replica of the incoming carrier signal. PLL has three basic components:-
1-Phase detector: is a device that produce a measure of the difference in phase between an incoming signal and the local replica. As the incoming signal and the local replica change with respect to each other, the phase difference (or phase error) becomes a time varying signal into the loop filter.

2-Loop filter: is the device governs the PLL response to these variations in the error signal.

3-VCO: is the device that produces the carrier replica. The VCO is a sinusoidal oscillator whose frequency is controlled by a voltage level at the device input.

In fig(13.1), the phase detector is shown as a multiplier, the loop filter is described by its impulse response function $f(t)$, with Fourier transform $F(\omega)$, and the voltage controlled oscillator (VCO) is also indicated. A VCO is an oscillator whose output frequency is a linear function of its input voltage over a certain range.

The output of VCO may be a digital signal (i.e not a sinusoidal), but it may be implemented as a read only memory whose output
frequency controlled by a combination of a clock and the error
signal (as a variable address).

- Let us consider the input signal to the PLL is given by

\[ r(t) = 2 \cos(\omega_c t + \theta(t)) \] \hspace{1cm} (13.1a)

Where \( \omega_c \) is the nominal carrier frequency and \( \theta(t) \) is a slowly
varying phase. Similarly, consider a normalized VCO output of the
form.

\[ x(t) = \sin(\omega_c t + \hat{\theta}(t)) \] \hspace{1cm} (13.1b)

Where \( \hat{\theta}(t) \) is the estimated phase.

These signals will produce an output error signal at the phase
detector output of the form

\[ e(t) = x(t)r(t) = 2 \sin[\omega_0 t + \hat{\theta}(t)] \cos[\omega_0 t + \theta(t)] \]
\[ = \sin[\theta(t) - \hat{\theta}(t)] + \sin[2\omega_0 t + \theta(t) + \hat{\theta}(t)] \] \hspace{1cm} ......(13-1c)

Assuming that the loop filter is low pass filter, the second term will
be filtered out. Thus the low pass filter provides error signal that is
a function of the difference phases between input and the output,
only.

This error signal is applied to the input VCO.

- The VCO output frequency is the time derivative of the of the
argument (angle) of the sine function in eq(13.1b).

- If we assume that \( \omega_c \) is the output frequency of the VCO when the
voltage is zero, we can express the difference in the VCO output
frequency from \( \omega_c \) as the differential of the phase term \( \hat{\theta}(t) \).
Therefore, since an input voltage of zero produces an output frequency of \( \omega_r \), the difference in the output frequency form \( \omega_r \) will be proportional to the value of the input voltage \( y(t) \).

\[
\Delta \omega(t) = \frac{d}{dt} \left[ \hat{\omega}(t) \right] = K_0 y(t) \quad \text{.........(13.2 a)}
\]

\[
= K_0 e(t) \ast f(t) \quad \text{.........(13.2 b)}
\]

\[
\approx K_0 \left[ \theta(t) - \hat{\theta}(t) \right] \ast f(t) \quad \text{.........(13.2 c)}
\]

\[
\sin \theta \approx \theta \quad \text{if } \theta \text{ is small}
\]

Where \( \Delta \omega(t) \)=the frequency difference

*=the convolution

\( K_0 \)=the gain of the VCO

\( f(t) \)=the loop filter impulse response

\[
\text{fig(13.1)}
\]

This linear differential equation in \( \hat{\theta}(t) \) (if small angle approximation) is known as the linearized loop equation. It is used to determine the loop behaviour during normal operation (where the phase error is small).

-Consider the Fourier transform of eq(13.2)
\[
\frac{d[\hat{\theta}(t)]}{dt} = F \left\{k_c \left[\theta(t) - \hat{\theta}(t)\right] \cdot f(t)\right\}
\]

\[j W \hat{\theta}(\omega) = K_0 \left[\theta(\omega) - \hat{\theta}(\omega)\right] F(\omega) \quad \text{.......(13.3)}\]

\[\hat{\theta}(\omega) \left[j \omega + K_0 F(\omega)\right] = K_0 \theta(\omega) F(\omega)\]

\[\frac{\hat{\theta}(\omega)}{\theta(\omega)} = \frac{K_0 F(\omega)}{j \omega + K_0 F(\omega)} = H(j \omega) \quad \text{.......(13.4)}\]

Where H(j\omega) is the closed loop transfer function of the PLL

**Ex13.1**

Show that for appropriately chosen \(k_c\), \(k_c\) and \(f(t)\) the linearized loop equation (for PLL) demonstrates a tendency toward phase lock—that is, the phase difference between the incoming signal and the VCO output tends to decrease.

**Solution**

\[\Delta \omega(t) \approx K_0 \left[\theta(t) - \hat{\theta}(t)\right] \cdot f(t) \quad \text{.......(13.3)}\]

1-Consider the case where the phase of the input signal \(\theta(t)\) is slowly varying with time.

2-If the phase difference on the right hand side of eq(13.3) is positive [i.e \(\theta(t) > \hat{\theta}(t)\)], so that \(\hat{\theta}(t)\) will increase with time, which will tend to reduce the magnitude of the difference \(\theta(t) - \hat{\theta}(t)\).

3-If \(\theta(t) = \hat{\theta}(t)\), then eq(13.3) indicates that \(\hat{\theta}(t)\) will not change with time, and the equality will be maintained.
Steady state tracking characteristics.

By using eq(13.4), we can obtain an expression for the Fourier transform of the phase error $E(\omega)$

$$\frac{\hat{\theta}(\omega)}{\theta(\omega)} = \frac{K_0 F(\omega)}{j\omega + K_0 F(\omega)} = H(j\omega) \quad \text{ ....(13.4)}$$

$$E(\omega) = \varphi(t) = \theta(\omega) - \hat{\theta}(\omega) = [1 - H(\omega)]\hat{\theta}(\omega)$$

$$E(\omega) = \frac{j\omega \theta(\omega)}{j \omega + K_0 F(\omega)} \quad \text{ ...(13.5)}$$

eq(13.5) can be used to determine the steady state error response of a loop to a variety of possible input characteristics. The steady state error is the residual error after all transients have died away.

PLL performance in noise

Reconsider the basic PLL shown in fig (13.1) with narrowband additive Gaussian noise $n(t)$, the expression for the input becomes

$$r(t) = \cos(\omega_t) + n(t)$$
Let us consider the input phase offset, $\theta$ to be constant.

The noise process $n(t)$, assumed to be a zero mean a narrowband Gaussian process, can be expressed into quadature components about the carrier frequency.

$$n(t) = n_c(t) \cos \omega_0 t + n_s(t) \sin \omega_0 t \quad \text{........}(13.6)$$

The output of the phase detector can be written as:

$$e(t) = x(t) r(t)$$

$$= \sin(\omega t + \hat{\theta}) \left[ \cos(\omega t + \hat{\theta}) + n_c(t) \cos \omega t + n_s(t) \sin \omega t \right]$$

As before, the loop filter eliminates the twice carrier frequency ($2\omega_0$) terms. Denoting the second and third terms of eq(13.7) as

$$\dot{n}(t) = n_c(t) \cos \hat{\theta} + n_s(t) \sin \hat{\theta} \quad \text{(13.8)}$$

Consider the auto correlation function of $\dot{n}(t)$

$$R(t_1, t_2) = R\{n_c(t_1) \cos \theta + n_s(t_1) \sin \theta \mid n_c(t_2) \cos \theta + n_s(t_2) \sin \theta \}$$
(13.9)

Where $E[.]$ denotes the expected value.
The cross terms on the right hand side of eq(13.9) are equal to zero because $n_s$ and $n_c$ are mutually independent and have zero means.
Eq(13.9) can be written as:

$$R(\tau) = R_c(\tau) \cos^2 \hat{\theta} + R_s(\tau) \sin^2 \hat{\theta} \quad ....(13.10)$$

Where $\tau = t_1 - t_2$. Taking Fourier transforms, the power spectral density of $\hat{n}(t)$ is seen to be

$$G(\omega) = \mathcal{F}[R(t)]$$

$$= G_c(\omega) \cos^2 \hat{\theta} + G_s(\omega) \sin^2 \hat{\theta} \quad ....(13.11)$$

Where $G_c(\omega)$ and $G_s(\omega)$ are the Fourier transforms of $R_c$ and $R_s$ respectively. But from eq(13.6), it can be seen that the spectra $G_c(\omega)$ and $G_s(\omega)$ are made of shifted versions of the spectra of the original noise process $n(t)$. Therefore, because

$$G_s(\omega) = G_c(\omega) = G_n(\omega_0 - \omega) + G_n(\omega_0 + \omega) \quad .....(13.12)$$

Where $G_n(\omega)$ is the spectral density of the original bandpass noise process $n(t)$. Equation(13.11) can be rewritten as

$$G(\omega) = [G_n(\omega - \omega_c) + G_n(\omega + \omega_c)] \cos^2 \hat{\theta} + [G_n(\omega - \omega_c) + G_n(\omega + \omega_c)] \sin^2 \hat{\theta}$$

$$\therefore G(\omega) = G_n(\omega - \omega_c) + G_n(\omega + \omega_c) \quad (13.13)$$
For the special case of white noise, we have \( G_n(\omega) = \frac{N_0}{2} \) watts/ Hz, where \( N_0 \) is the signal sided spectral density of the white noise. Thus from Eq(13.13), for this special case

\[
G(\omega) = \frac{N_0}{2} + \frac{N_0}{2} = N_0 \quad \text{......(13.14)}
\]

- The spectral density of the VCO phase, \( \vartheta \), is related to the spectral density of the noise process through the loop transfer function (eq13.4)

\[
G_\vartheta(\omega) = G(\omega) |H(\omega)|^2 \quad \text{..........(13.15)}
\]

where

\[
G(\omega) = G_n(\omega - \omega_0) + G_n(\omega + \omega_0) \quad \text{......(13.13)}
\]

\[
H(\omega) = \frac{K_0 F(\omega)}{K_0 F(\omega) + j \omega} \quad \text{..........(13.4)}
\]

The variance of the output phase is then

\[
\sigma_\vartheta^2 = \frac{1}{2\pi} \int_{-\infty}^{\infty} G(\omega) |H(\omega)|^2 d\omega \quad \text{..........(13.16)}
\]

For special case of white noise

\[
\sigma_\vartheta^2 = \frac{N_0}{2\pi} \int_{-\infty}^{\infty} |H(\omega)|^2 d\omega \quad \text{......(13.17)}
\]

The integral in eq(13.17) is called the two sided loop bandwidth \( W_L \). The single sided loop bandwidth is termed \( B_L \). The definitions of these terms are

\[
W_L = 2B_L = \frac{1}{2\pi} \int_{-\infty}^{\infty} |H(\omega)|^2 d\omega \text{ Hertz} \quad \text{......(13.18)}
\]
Thus if the noise process is white and the small angle approximation holds, the phase variance is given by

$$\sigma^2 = 2N_0B_L$$

The phase variance \( \sigma^2 \) is a measure of the amount of jitter in the VCO output due to noise at the input. Eq(13.19) and Eq(13.5) \( [E(\omega)=j\omega\theta(\omega)/K_0 (w)/K_0F_0(\omega)+j\omega] \) highlight one of many tradeoffs in communication theory. If \( \sigma^2 \) is small, the loop bandwidth is small. But the narrower the bandwidth of \( H(\omega) \), the poorer will be the loop ability to track incoming signal phase response.

**Suppressed of carrier loops**

In the case of a phase modulation, if the carrier phase variation due to the modulation less than \( \pi/2 \) radians, there will be positive energy at the carrier frequency. This is called a system design that has a residual carrier component. A diagram of the signal space for a binary phase modulated with a residual carrier components is shown in fig(13.2), for modulating angle of \( \gamma \leq \pi/2 \). However, the residual component is wasted energy, it is not to transmit the information, only to transmit the carrier. Thus most modern phase modulated systems are suppressed carrier systems. This means that there is no average energy transmitted at the carrier frequency also there is no longer any signal for the basic PLL of fig(13.1) to track.
Consider, as an example, a BPSK

\[ r(t) = m(t) \sin (\omega_0 t + \theta) + n(t) \]

where \( m(t) = \pm 1 \) with equal probability. This is suppressed carrier with the average energy at radian frequency \( \omega_0 \) is zero. This represented graphically in fig (13.2) when \( \gamma = \pi / 2 \), and in this case the residual carrier will vanish.

To acquire and track the phase of the carrier, the effects of the modulation must be eliminated. One way to eliminate the modulation is to square the signal.

\[ r^2(t) = m^2(t) \sin^2 (\omega_0 t + \theta) + n^2(t) + 2 n(t) m(t) \sin (\omega_0 t + \theta) \]

\[ = \frac{1}{2} \left( \frac{1}{2} - \frac{1}{2} \cos (2 \omega_0 t + 2\theta) \right) + n^2(t) + 2 n(t) m(t) \sin (\omega_0 t + \theta) \]

(13.20)

If \( m^2(t) = 1 \), the second term on the right hand side of eq(13.20) is a carrier related term (at twice the original carrier frequency) that can be acquired and tracked with a basic PLL of the type illustrated.
in fig(13.1). Such an arrangement is illustrated in fig(13.3). The problems with this schematic are:-

a) All phase angles have been doubled. Thus, the phase noise and phase jitter have been doubled.

b) Larger S/N is required for this PLL to overcome this larger internal variation of the noise.

c) False lock. This additional loss due to the terms in eq(13.20)

\[ n^2(t) + 2n(t)m(t) \sin (\omega_0 t + \theta) \]

is called the loop squaring loss \((S_L)\) is given by

\[
\frac{S_L}{S} \leq 1 + \frac{(N \cdot B_i)}{S} \tag{13.20}
\]

Where \(S\) is the signal power

\(B_i\) is the filter bandwidth

\(N_o\) is the single sided power spectral density of the prefiltered, white Gaussian noise process.

Fig (13.3)

Eq(13.20) can be expressed as
\[ \therefore \frac{S_L}{S} \leq 1 + \frac{1}{2P_i} \quad \text{(13.21)} \]

Where \( P_i \) is the signal to noise ratio

**Costas loop**

- Fig (13.4) shows the Costas loop. This loop design is important because it eliminates the square law device, which can be difficult to implement at carrier frequencies, and replaces it with a multiplier and relatively simple low pass filters. The problem in this loop is to implement the two LPF identical. This problem can be solved by using the digital filter.

- The decision as to whether to implement a Costas loop or the classical design of fig(3.3) amounts to a design decision between the difficulty of implementing the squaring device and the difficulty of implementing closely matched arm filters.

![Costas Loop Diagram](image)

**Higher order suppressed carrier loops**
-Sequaring the signal a second time (equivalent to taking the original signal to the fourth power) can be seen to produce a term with a carrier component at four times the transmuted carrier’s frequency. The loss for fourth power loop is

\[ S_L \leq 1 + \frac{9}{\rho_i} + \frac{6}{\rho_i^2} + \frac{3}{2\rho_i^3} \]  

(13.22)

**Ex13.2**

Compare and discuss the results of the upper bounds on squaring loss \((S_L)\) for second and forth loops (used for receiver synchronization) if the input loop signal to noise ratio \((P_i)\) is 10 dB.

**Solution :**

\[
10\text{dB}=10\log \frac{S}{N} \quad \therefore \frac{S}{N}=10=P_i
\]

For the squaring loop:

\[
S_L = 1 + \frac{1}{2P_i} = 1 + \frac{1}{2 \times 10} = 1.05
\]

\[=10\log1.05=0.2\text{dB}\]

For the fourth loop:

\[
S_L = 1 + \frac{9}{P_i} + \frac{6}{P_i^2} + \frac{3}{2P_i^3}
\]

\[= 1 + \frac{9}{10} + \frac{6}{10^2} + \frac{3}{2(10^3)}\]

\[=1+0.9+0.06+0.0015\]

\[=10\log1.9615=2.9\text{dB}\]
Thus, an input signal to noise ratio of 10dB is suitable to keep losses small for the squaring loop, the same signal to noise ratio may allow significant losses for the fourth power loop.

**Nonlinear loop**

- The linearized model is shown in fig(13.5). The model makes use of the small angle approximation.

\[
\sin (\theta - \hat{\theta}) \approx \theta - \hat{\theta}
\]

(13.20)

This model is accurate when the loop is in lock and performing as desired (small phase error).

- When the small angle approximation is inaccurate, an appropriate model is the shown in fig(13.6) which is called the nonlinearized PLL mode.
Fig(13.6) Schematic nonlinearized PLL model

**Acquisition**

Every loop must acquire lock—that is, it must be brought into lock. Acquisition can be accomplished with aid of external circuits or signals (aided acquisition) or in some cases by an unaided PLL (self acquisition).

Let us consider noise free, first order loop as shown in fig(13.6) where \( h(t) = 0 \) (noise free) and \( F(\omega) = 1 \) first order.

Let the input phase \( \dot{\theta}_i(t) = \omega_i(t) \)

And the output phase

\[
\dot{\theta}_o(t) = \omega_o(t) + \int_0^t k_s \sin \alpha(t) dt + \dot{\theta}(\omega)
\]

(13.21a)

Where \( \omega_i \) and \( \omega_o \) are the radian frequencies of the input and the output signals, respectively. Thus the phase error is given by

\[
e(t) = \theta_i(t) - \theta_o(t)
\]

(13.21b)

\[
e(t) = \omega_i(t) - \omega_o(t) - \int_0^t k_s \sin e(t) dt + \dot{\theta}(\omega)
\]

Differentiating both sides and letting \( \Delta \omega = \omega_i - \omega_o \).
\[
\frac{de(t)}{dt} = \Delta \omega - k \cdot \sin(t) \tag{13.22}
\]

Eq(13.22) describes the behavior of the first order noise free PLL. The loop being in lock requires that \(
\frac{de(t)}{dt} = 0
\) \tag{13.23}

Eq(13.23) is a necessary, but not a sufficient condition for phase lock. This can be verified by observing the phase plane diagram of fig(13.7).

\[
\frac{de(t)}{dt} = \Delta \omega - k \cdot \sin(t) \tag{13.22}
\]

1-Observe point a, if the phase error is displaced a little to the left or right of point a, the sign of the derivative term is such that the phase error Fig(13.7) back toward a. Thus point a is a stable point of the system and the lock can be obtained and maintained.
2-Now consider the case of point b, if the phase error is exactly at b, eq(13.23)\([d\varepsilon(t)/dt=0]\).
If there is any slight offset from b, the sign of the derivative term will be such that the error will be driven away from b and the loop is not lock.
3-The amount of time required for loop to come into lock can be a very important system design consideration.
4-by observing eq(13.22,13.23), we can see that the requirement of eq(13.23) for phase lock cannot met unless
\[
\frac{|\Delta \omega|}{|K_0|} \leq 1 \quad \frac{d\varepsilon}{dt} = \Delta \omega - K_0 \sin \varepsilon
\] (13.22)
\[
\frac{d\varepsilon}{dt} = 0
\] (13.23)
This is because sinusoidal functions have a maximum amplitude of unity. This range of the frequency difference \(-k_* \leq \Delta \omega \leq k_*\) is sometimes called the lock in range of the loop.
5-If a loop is unable to track out all phase errors, the received symbol error probability will degraded relative to what is theoretically achievable.
6-Symbol synchronization.
a-It should be pointed that symbol synchronization and bit synchronization are used interchangeably in the literature:
1-If the system is coded, one uses a symbol synchronizer.
2-If the system is not coded, one uses a bit synchronizer.
b-To find the optimum procedure to estimate symbol-stream–
derived bit synchronization.

c-Fig (13.8) shows a typical symbol sequence.

1-The symbols are shown grouped in units of eight to form a
word.

2-Aframe is composed of N words (N integer).

![Diagram showing symbol sequence and frame structure]

fig (13.3)

-All digital receivers need to be synchronized to the incoming
digital symbol transitions in order to achieve optimum
demodulation. There are two classes of synchronizers based on the
known information about data stream:-

1-Non data aided synchronizer (NDA): This type of the
synchronizer do not know information about the actual data
sequence.

2-Data aided synchronizers(DA): This type of synchronizer use
known information about data stream.

The symbol synchronizers can be classified into two basic groups
according to the type of the loop:-
1-Open loop synchronizers: These circuits recover a replica of the transmitter data clock output directly from operation on the incoming data stream.

2-Closed loop synchronizers: These synchronizers attempt to lock a local data clock to the incoming signal by use of comparative measurements on the local and incoming signals.

1-Open loop symbol synchronizers
-Open loop symbol synchronizers are also called filter synchronizers.
-This class of synchronizers generates a frequency component at the symbol rate by operating on the incoming baseband sequence with a combination of filtering and a nonlinear device.
-In this synchronizer, the desired frequency component, at the data symbol rate, is filtered by the bandpass filter, and shaped with a high gain saturating amplifier. The shaping recovers the square wave appearance of the data clock signal.
-Three examples of open loop bit synchronizers are shown in fig(13.9):-
1-In the first example fig(3.9a) the incoming signal (s) is filtered with matched filter and rectified by the square device. The output waveform from square law device will contain a Fourier component at the fundamental frequency of the data clock. This frequency is filtered by BPF and shaped with an ideal saturating amplifier, with transfer function (sigum function)

\[
Sgn(t) = \begin{cases} 
1 & t > 0 \\
0 & t = 0 \\
-1 & t < 0 
\end{cases}
\]

2-the second example shown in fig(13.9b) produces a Fourier component at the data clock frequency by means of a delay and
multiply. The delay show in fig(13.9b) is half a bit period, which is the best value because it provides the strongest Fourier component.

3-The third example shown in fig (13.9c). The main operations are those differentiation and rectification by using a square law device. For a square wave input, the differentiator will produce positive or negative spikes at all symbol (bit) transitions. when rectified, the resulting sequence of positive spikes will have a Fourier component at the data symbol (bit) rate.

**Closed loop symbols synchronizers**

- The primary disadvantage of open loop symbol synchronization methods is that there is an unavoidable non-zero mean tracking. Closed loop, symbol data synchronizers use comparative measurements on the incoming signal and a locally generated data lock signal to bring the locally generated signal into synchronism with incoming data transitions.

- The most popular of the closed loop symbol synchronizers is the early/late gate synchronizer as shown in fig(13.10).

- The synchronizer operates by performing two separate integrations of the incoming signal energy over two different(T-d) second portions of a symbol interval. The first integration (the early gate) begins from zero to T-d. The second integration (the late gate) begins from d to T. The difference in the absolute values of the outputs of these two integrations \( \mathcal{Y}_1 \) and \( \mathcal{Y}_2 \) is a measure of the receiver’s symbol timing error, and it can be fed back to the loop’s
timing reference to correct loop timing. Fig(13.11) shows the receiver timing symbol.

The action of the early/late gate synchronizer can be summarized as follow:-

1-In the case of perfect synchronization as shown in fig(13.11a), both gates within a signal symbol interval. Both integrators will accumulate the same of signal and their difference (error signal) $e=0$.

![Early/late-gate data synchronizer](image)
2-the case shown in fig(13.11b) is for a receiver whose data clock is early relative to the incoming data:

a-the late gate integrator will accumulate signal over its entire (T-d) integration interval.

b-the early gate integrator will accumulate signal over \([T-d-2\Delta]\) where \(\Delta\) is the portion of the early gate interval falling in the previous bit interval.

Thus the error signal in this case \(e \alpha 2\Delta\)

**Frame synchronization**

All digital data streams have some sort of frame structure. The data streams is organized into uniformly sized groups of bit as shown previously. Computer data are typically organized into words of some number of 8 bit bytes.
to receive the incoming data stream, the receiver needs to be synchronized with the data stream’s frame structure.

Frame synchronization is usually accomplished with the aid of some special signaling procedure from the transmitter.

The simplest frame synchronization aid is the frame marker shown in fig (13.12). The frame marker is a single bit or a short pattern of bits that the transmitter injects periodically into the data stream. The receiver, having achieved data synchronization, correlates the known pattern with the incoming data stream at the known injection interval.

The advantage of the frame marker is its simplicity. Even a single bit can suffice as a frame marker if a sufficient number of correlations are accumulated before deciding whether or not the system has achieved synchronization. The major drawback is that
the sufficient number may be very large and thus the expected time required to acquire synchronization would be long. Therefore, frame markers are most useful in systems that transmit data continuously, like may telephony and computer links.

**Network synchronization**

- For systems using coherent modulation techniques, one direction communication such as most microwave links, land line links or fiber optics links, the synchronization architecture is performed at the receiver.

- For systems using noncoherent modulation techniques or that involves many user accessing a central communication node, such as many satellite communication systems, the synchronization is performed at a terminal transmitter. This means that the terminal transmitter parameters are modified to achieve synchronization rather than modifying the central nodes receiver parameters. This approach is used for time division multiple access (TDMA). In TDMA each user is allotted a segment of time in which to transmit its information. The terminal transmitter must be synchronized with the system in order for its transmitted burst data to arrive at the central node at the time when the node is prepared to receive the data.

- Synchronization of the terminal transmitter also makes sense with systems that combine signal processing at the central node with frequency division multiple access (FDMA)
-If the terminals precorrect their transmission to be synchronized with the central node, the node can use a fixed set of channel filters and a single timing reference for the processing of all channels. Otherwise, the node would require a separate time and frequency acquisition and tracking capability for each incoming channel.

It seems clear that terminal transmitter synchronization is often more reasonable system approach to synchronizing network.

Transmitter synchronization procedures may be classified being either open loop or closed loop;-  
1-Open loop techniques do not depend on any measurement of the arriving signal parameters at the central node. The terminal precorrect its transmission based on stored knowledge of link parameters that have been provided by some external authority but may possibly be modified by observations of a return signal from the central node. Open loop techniques depend on link parameters being accurately known.

The main advantages of the open loop methods are that acquisitions is fast the procedure can work without a return link and the amount of real time computation that is required is small. The disadvantages of the open loop methods are that they require knowledges of the required link parameters variation. 
2-Closed loop techniques involve measurements of the synchronization accuracy of the incoming transmission from the terminal upon that their arrival at the central node, and the return of
the results of these measurements to the terminal via a return path. Thus, closed loop methods require a return path that provides a response to the terminal’s transmissions, the ability in the terminal to recognize the response for what it is, and the ability in the terminal to modify the transmitter characteristics based on the response. The advantages of the closed loop are that no external source of knowledge is required for the system to work and the responses on the return link allow the system adapt easily and quickly to changing the characteristics. The disadvantages of closed loop methods are that they require a large amount of the real time processing and require two way links to every terminal.

Ex13.3 Shows that the loop bandwidth of a first order phase locked loop is given by

\[ B_L = \frac{K_0}{4} \text{ where } K_0 \text{ is the loop gain} \]

**solution**

The loop bandwidth is given by eq(13.18)

\[ 2B_L = \frac{1}{2\pi} \int_{-\infty}^{\infty} |H(j\omega)|^2 d\omega \]

where from eq (13.4)

\[ H(j\omega) = \frac{K_0F(\omega)}{j\omega+K_0F(\omega)} \]

for a first order loop F(\(\omega\)) = 1
\[ H(j\omega) = \frac{K_0}{j\omega + k_0} \]
\[ |H(j\omega)|^2 = \frac{K^2}{\omega^2 + K_0^2} \]

\[ 2B_L = \frac{1}{2\pi} \int_{-\infty}^{\infty} \frac{K_0^2}{\omega^2 + K_0^2} \, d\omega = \frac{1}{2\pi} \int_{-\infty}^{\infty} \frac{d\omega}{\omega^2 + K_0^2} \]

\[ = \frac{1}{2\pi} \int_{-\infty}^{\infty} \frac{K_0^2 \, d\omega}{K_0^2} \left( \frac{\omega^2}{K_0^2} + 1 \right) = \frac{1}{2\pi} \int_{-\infty}^{\infty} \frac{d\omega}{\omega^2 + K_0^2 + 1} \]

Let \( x = \frac{\omega}{K_0} \)
\[ \therefore dx = \frac{d\omega}{K_0} \]

\[ 2B_L = \frac{K_0}{2\pi} \int_{-\infty}^{\infty} \frac{dx}{x^2 + 1} = \frac{K_0}{2\pi} \left[ \arctan x \right]_{-\infty}^{\infty} \]

\[ 2B_L = \frac{K_0}{2\pi} \left[ \frac{\pi}{2} - \left( -\frac{\pi}{2} \right) \right] = \frac{K_0}{2} \]

\[ \therefore B_L = \frac{K_0}{4} \]