Experiment No.12
Field Effect Transistor (FET)

OBJECT:
To investigate the FET characteristics.

APPARATUS:
1-D.C power supply.
2-Oscilloscope, A.V.Ometer.
3-FET, Resistors 1 kΩ and 200 kΩ.

THEORY
The acronym 'FET' stands for field effect transistor. It is a three-terminal unipolar solid-state device in which current is controlled by an electric field as is done in vacuum tubes. Broadly speaking, there are two types of FETs:
(a) junction field effect transistor (JFET)
(b) metal-oxide semiconductor FET (MOSFET)
It is also called insulated-gate FET (IGFET). It may be further subdivided into:
(i) depletion-enhancement MOSFET i.e. DEMOSFET
(ii) enhancement-only MOSFET i.e. E-only MOSFET
Both of these can be either P-channel or N-channel devices.

As shown in Fig.1, it can be fabricated with either an N-channel or P-channel though N-channel is generally preferred. For fabricating an N-channel JFET, first a narrow bar of N-type semiconductor material is taken and then two P-type junctions are diffused on opposite sides of its middle part [Fig.1 (a)]. These junctions form two P-N diodes or gates and the area between these gates is called channel. The two P-regions are internally connected and a single
lead is brought out which is called gate terminal. Ohmic contacts (direct electrical connections) are made at the two ends of the bar—one lead is called source terminal S and the other drain terminal D. When potential difference is established between drain and source, current flows along the length of the ‘bar’ through the channel located between the two P-regions. The current consists of only majority carriers which, in the present case, are electrons. P-channel JFET is similar in construction except that it uses P-type bar and two N-type junctions. The majority carriers are holes which flow through the channel located between the two N-regions or gates.

Following FET notation is worth remembering:

1. Source. It is the terminal through which majority carriers enter the bar. Since carriers come from it, it is called the source.
2. Drain. It is the terminal through which majority carriers leave the bar i.e. they are drained out from this terminal. The drain to source voltage $V_{DS}$ drives the drain current $I_D$.
3. Gate. These are two internally-connected heavily-doped impurity regions which form two P-N junctions. The gate-source voltage $V_{GS}$ reverse biases the gates.
4. Channel. It is the space between two gates through which majority carriers pass from source-to-drain when $V_{DS}$ is applied.

Schematic symbols for N-channel and P-channel JFET are shown in Fig.1 (c). It must be kept in mind that gate arrow always points to N-type material.

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**Fig. 1 FET construction**
**Static Characteristics of a JFET**

We will consider the following two characteristics:

(i) drain characteristic: It gives relation between $I_D$ and $V_{DS}$ for different values of $V_{GS}$ (which is called running variable).

(ii) transfer characteristic: It gives relation between $I_D$ and $V_{GS}$ for different values of $V_{DS}$.

We will analyze these characteristics for an N-channel JFET connected in the common-source mode as shown in Fig. 2. We will first consider the drain characteristic when $V_{GS} = 0$ and then when $V_{GS}$ has any negative value upto $V_{GS} (off)$.

![Fig. 2 JFET Drain Characteristic With $V_{GS} = 0$](image)

**JFET Drain Characteristic With $V_{GS} = 0$**

Such a characteristic is shown in Fig. 3.

It can be subdivided into following four regions:

1. Ohmic Region OA: This part of the characteristic is linear indicating that for low values of $V_{DS}$, current varies directly with voltage following Ohm's Law. It means that JFET behaves like an ordinary resistor till point A (called knee) is reached.

2. Curve AB In this region, $I_D$ increases at reverse square-law rate upto point B which is called pinch-off point. This progressive decrease in the rate of increase of $I_D$ is caused by the square law increase in the depletion region at each gate upto point B where the two regions are closest without touching each other.

![Fig. 3](image)
3. Pinch-off Region BC: It is also known as saturation region or ‘amplified’ region. Here, JFET operates as a constant-current device because $I_D$ is relatively independent of $V_{DS}$. It is due to the fact that as $V_{DS}$ increases, channel resistance also increases proportionally thereby keeping $I_D$ practically constant at $I_{DSS}$. It should also be noted that the reverse bias required by the gate-channel junction is supplied entirely by the voltage drop across the channel resistance due to flow of $I_{DSS}$ and none by external bias because $V_{GS} = 0$.

4. Breakdown Region: If $V_{DS}$ is increased beyond its value corresponding to point C (called avalanche breakdown voltage), JFET enters the breakdown region where $I_D$ increases to an excessive value. This happens because the reverse-biased gate-channel P-N junction undergoes avalanche breakdown when small changes in $V_{DS}$ produce very large changes in $I_D$. It is interesting to note that increasing values of $V_{DS}$ make a JFET behave first as a resistor (ohmic region), then as a constant-current source (pinch-off region) and finally, as a constant-voltage source (breakdown region).

**Procedure:**
1. Connect the circuit as shown in fig 4.
2. Let $V_{DS} = (0, 0.5, 1, 1.5, 2, 2.5, 3, 4, 5)$ V measure $I_D$.
3. Repeat step 3 for $V_{GS} = (0.5, 1, 1.5, 2, 2.5, 3, 3.5, 4, 4.5)$ V.

**REQUIREMENTS:**
1. Draw (drain characteristics) between $I_D$ & $V_{DS}$ for different values of $V_{GS}$.
2. Draw $I_D$ with $V_{GS}$ & find $g_m$.

**DISCUSSION:**
1. Comment on your results.
2. Compare between the transistor & FET.
3. What are the kind of FET.