TRANSITION AND DIFFUSION CAPACITANCE:-

Electronic devices are inherently sensitive to very high frequencies. Most shunt capacitive effects that can be ignored at lower frequencies because the reactance $X_C = 1/2\pi$ fC is very large (open-circuit equivalent). This, however, cannot be ignored at very high frequencies. X_C will become sufficiently small due to the high value of f to introduce a low-reactance "shorting" path. In the p-n semiconductor diode, there are two capacitive effects to be considered. Both types of capacitance are present in the forward- and reverse-bias regions, but one so outweighs the other in each region that we consider the effects of only one in each region.

In the reverse-bias region we have the transition- or depletion-region capacitance (C_T), while in the forward-bias region we have the diffusion (C_D) or storage capacitance.

Recall that the basic equation for the capacitance of a parallel-plate capacitor is defined by C =εA/d, where ε is the permittivity of the dielectric (insulator) between the plates of area A separated by a distance d. In the reverse-bias region there is a depletion region (free of carriers) that behaves essentially like an insulator between the layers of opposite charge. Since the depletion width (d) will increase with increased reverse-bias potential, the resulting transition capacitance will decrease, as shown in Fig. 1.37. The fact that the capacitance is dependent on the applied reverse-bias potential has application in a number of electronic systems. In fact, diode will be introduced whose operation is wholly dependent on this phenomenon. Although the effect described above will also be present in the forward-bias region,

it is overshadowed by a capacitance effect directly dependent on the rate at which charge is injected into the regions just outside the depletion region. The result is that increased levels of current will result in increased levels of diffusion capacitance However, increased levels of current result in reduced levels of associated resistance (to be demonstrated shortly), and the resulting time constant (τ = RC), which is very important in high-speed applications, does not become excessive. The capacitive effects described above are represented by a capacitor in parallel with the ideal diode, as shown in Fig. 1.38. For low- or mid-frequency applications (except in the power area), however, the capacitor is normally not included in the diode symbol.
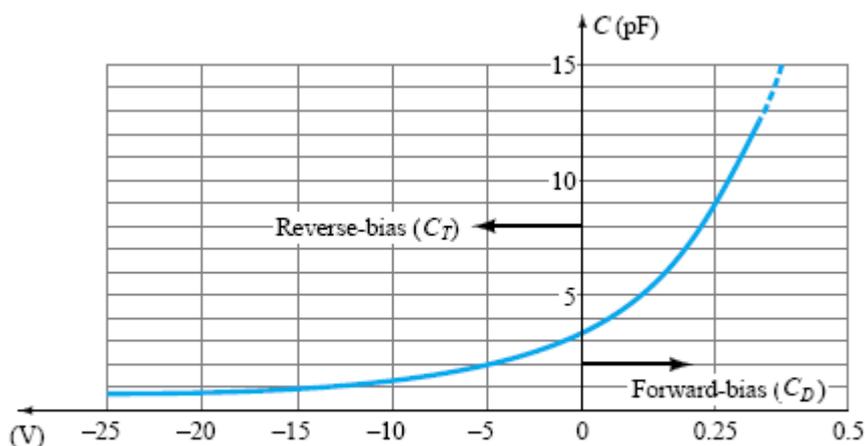

Figure 1.37 Transition and diffusion capacitance versus applied bias for a silicon diode.
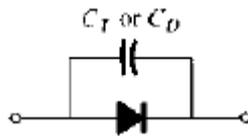
Figure 1.38 Including the effect of the transition or diffusion capacitance on the semiconductor diode.

SEMICONDUCTOR DIODE NOTATION:-

The notation most frequently used for semiconductor diodes is provided in Fig. 1.40.
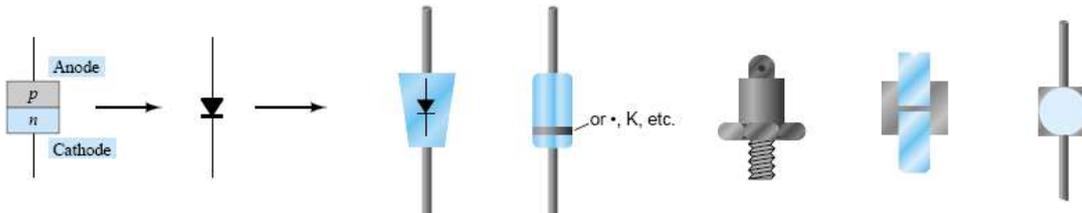

Figure 1.40 Semiconductor diode notation.

ZENER DIODES :-

The characteristic drops in an almost vertical manner at a reverse-bias potential denoted V_Z. The fact that the curve drops down and away from the horizontal axis rather than up and away for the positive V_D region reveals that the current in the Zener region has a direction opposite to that of a forward-biased diode. This region of unique characteristics is employed in the design of Zener diodes, which have the graphic symbol appearing in Fig. 1.48a. Both the semiconductor diode and zener diode are presented side by side in Fig. 1.48 to ensure that the direction of conduction of each is clearly understood together with the required polarity of the applied voltage. For the semiconductor diode the "on" state will support a current in the direction of the arrow in the symbol. For the Zener diode the direction of conduction is opposite to that of the arrow in the symbol as pointed out in the introduction to this section. Note also that the polarity of V_D and V_Z are the same as would be obtained if each were a resistive element.
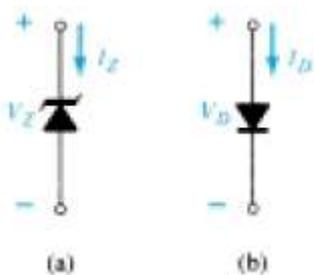

Figure 1.48 Conduction direction: (a) Zener diode; (b) semiconductordiode.

The location of the Zener region can be controlled by varying the doping levels. An increase in doping, producing an increase in the number of added impurities, will decrease the Zener potential. Zener diodes are available having Zener potentials of 1.8 to 200 V with power ratings from 1/4 to 50 W. Because of its higher temperature and current capability, silicon is usually preferred in the manufacture of Zener diodes. The complete equivalent circuit of the Zener diode in the Zener region includes a small dynamic resistance and dc battery equal to the Zener potential, as shown in Fig. 1.49. For all applications to follow, however, we shall assume as a first approximation that the external resistors are much larger in magnitude than the Zener-equivalent resistor and that the equivalent circuit is simply the one indicated in Fig. 1.49b. A larger drawing of the Zener region is provided in Fig. 1.50 to permit a description

of the Zener nameplate data appearing in Table 1.4 for a 10V, 500-mW, 20% diode. The term nominal associated with V_Z indicates that it is a typical average value. Since this is a 20% diode, the Zener potential can be expected to vary as 10 V , 20%.
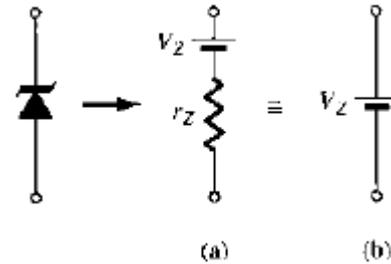

Figure 1.49 Zener equivalentcircuit: (a) complete; (b) approximate.
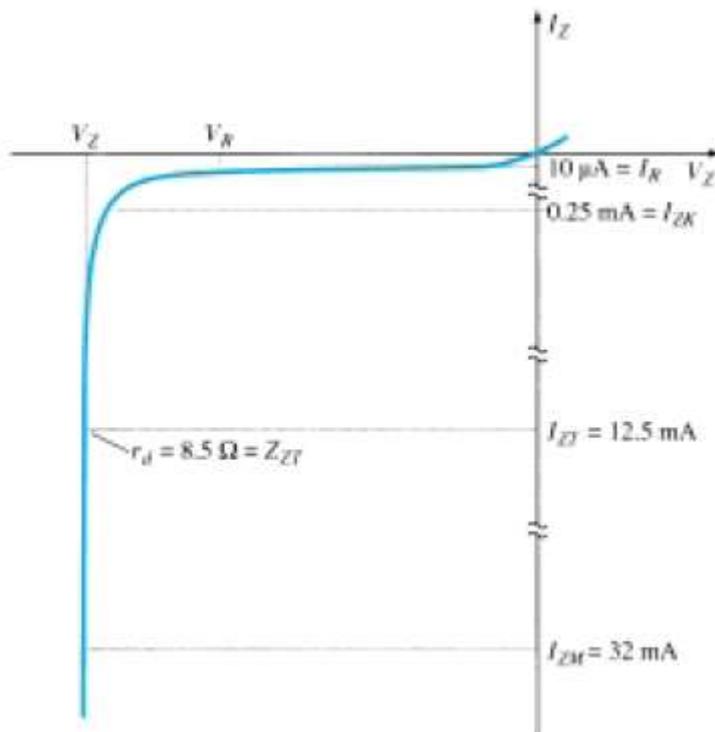

Figure 1.50 Zener test characteristics.

TABLE 1.4 Electrical Characteristics (25°C Ambient Temperature Unless Otherwise Noted)

Zener Voltage Nominal, V_Z (V)	Test Current, I_{ZT} (mA)	Max Dynamic Impedance, Z_{ZT} at I_{ZT} (Ω)	Maximum Knee Impedance, Z_{ZK} at I_{ZK} (Ω) (mA)		Maximum Reverse Current, I_R at V_R (μA)	Test Voltage, V_R (V)	Maximum Regulator Current, I_{ZM} (mA)	Typical Temperature Coefficient (%/°C)
10	12.5	8.5	700	0.25	10	7.2	32	+0.072

or from 8 to 12 V in its range of application. Also available are 10% and 5% diodes with the same specifications. The test current I_{ZT} is the current defined by the 1/4 power level, and Z_{ZT} is the dynamic impedance at this current level. The maximum knee impedance occurs at the knee current of I_{ZK}. The reverse saturation current is provided at a particular potential level, and I_{ZM} is the maximum current for the 20% unit.

<u>LIGHT-EMITTING DIODES :-</u>

As the name implies, the light-emitting diode (LED) is a diode that will give off visible light when it is energized. In any forward-biased p-n junction there is, within the structure and primarily close to the junction, a recombination of holes and electrons. This recombination requires that the energy possessed by the unbound free electron be transferred to another state. In all semiconductor p-n junctions some of this energy will be given off as heat and some in the form of photons. In silicon and germanium the greater percentage is given up in the form of heat and the emitted light is insignificant. In other materials, such as gallium arsenide phosphide (GaAsP) or gallium phosphide (GaP), the number of photons of light energy emitted is sufficient to create a very visible light source.

The process of giving off light by applying an electrical source of energy is called electroluminescence.

As shown in Fig. 1.54 with its graphic symbol, the conducting surface connected to the p-material is much smaller, to permit the emergence of the maximum number of photons of light energy. Note in the figure that the recombination of the injected carriers due to the forward-biased junction results in emitted light at the site of recombination. There may, of course, be some absorption of the packages of photon energy in the structure itself, but a very large percentage are able to leave, as shown in the figure.
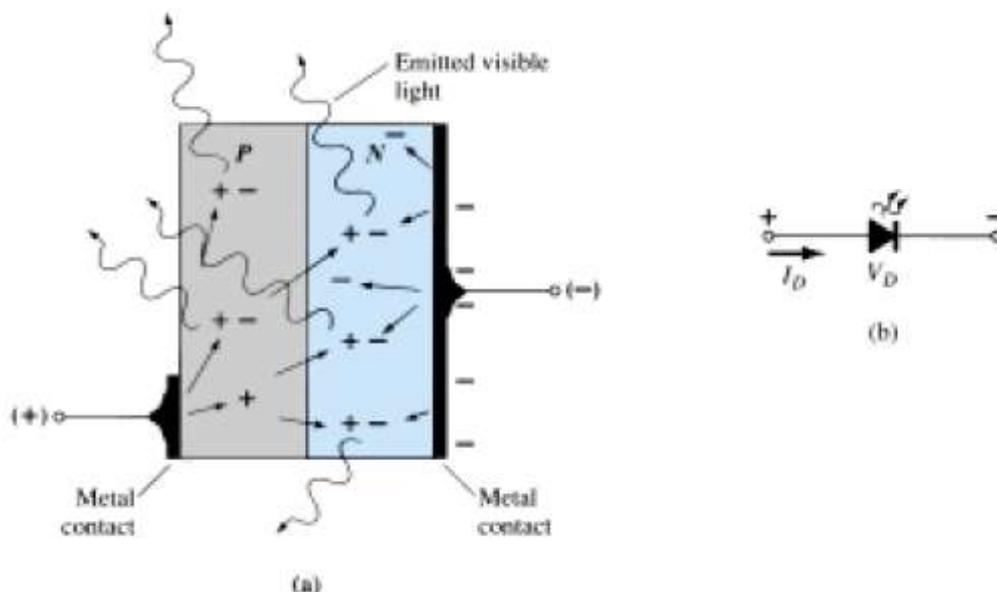

Figure 1.54 (a) Process of electroluminescence in the LED; (b) graphic symbol.

The appearance and characteristics of a subminiature high-efficiency solid-state lamp manufactured by Hewlett-Packard appears in Fig. 1.55. Note in Fig. 1.55b thatthe peak forward current is 60 mA, with 20 mA the typical average forward current. The test conditions listed in Fig. 1.55c, however, are for a forward current of 10 mA. The level of V_D under forward-bias conditions is listed as V_F and extends from 2.2 to 3 V. In other words, one can expect a typical operating current of about 10 mA at 2.5 V for good light emission.

Two quantities yet undefined appear under the heading Electrical/Optical Characteristics at $T_A = 25°C$. They are the axial luminous intensity (IV) and the luminous efficacy (ήv). Light intensity is measured in candela. One candela emits a light flux of 4π lumens and establishes an illumination of 1 footcandle on a 1-ft^2

area 1 ft from the light source. Even though this description may not provide a clear understanding of the candela as a unit of measure, its level can certainly be compared between similar devices. The term efficacy is, by definition, a measure of the ability of a device to produce a desired effect. For the LED this is the ratio of the number of lumens generated per applied watt of electrical energy. The relative efficiency is defined by the luminous intensity per unit current.

Since the LED is a p-n junction device, it will have a forward-biased characteristic similar to the diode response curves. Note the almost linear increase in relative luminous intensity with forward current.

Diode Applications :-

LOAD-LINE ANALYSIS :-

The applied load will normally have an important impact on the point or region of operation of a device. If the analysis is performed in a graphical manner, a line can be drawn on the characteristics of the device that represents the applied load. The intersection of the load line with the characteristics will determine the point of operation of the system. Such an analysis is, for obvious reasons, called load-line analysis.

Although the majority of the diode networks analyzed in this chapter do not employ the load-line approach, the technique is one used quite frequently in subsequent chapters, and this introduction offers the simplest application of the method. It also permits a validation of the approximate technique described throughout the remainder of this chapter.

Consider the network of Fig. 2.1 employing a diode having the characteristics of Fig. 2.1b. Note in Fig. 2.1 that the "pressure" established by the battery is to establish a current through the series circuit in the clockwise direction. The fact that this current and the defined direction of conduction of the diode are a "match" reveals that the diode is in the "on" state and conduction has been established. The resulting polarity across the diode will be as shown and the first quadrant (V_D and I_D positive) of Fig. 2.1 will be the region of interest—the forward-bias region. Applying Kirchhoff's voltage law to the series circuit will result in

$$E - V_D - V_R = 0$$

$$\boxed{E = V_D + I_D R} \qquad (2.1)$$

The two variables of Eq. (2.1) (VD and ID) are the same as the diode axis variables of Fig. 2.1b. This similarity permits a plotting of Eq. (2.1) on the same characteristics of Fig. 2.1b. The intersections of the load line on the characteristics can easily be determined if one simply employs the fact that anywhere on the horizontal axis ID = 0 A and anywhere on the vertical axis V_D = 0 V. If we set V_D = 0 V in Eq. (2.1) and solve for I_D, we have the magnitude of I_D on the vertical axis. Therefore, with VD = 0 V, Eq. (2.1) becomes
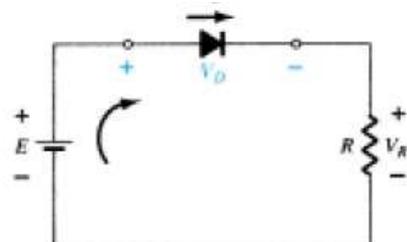
Figure 2.1 Series diode configuration:

$$E = V_D + I_D R$$
$$= 0 \text{ V} + I_D R$$

$$I_D = \frac{E}{R}\bigg|_{V_D=0 \text{ V}}$$ (2.2)

as shown in Fig. 2.2. If we set ID _ 0 A in Eq. (2.1) and solve for VD, we have the magnitude of VD on the horizontal axis. Therefore, with ID _ 0 A, Eq. (2.1) becomes

$$E = V_D + I_D R$$
$$= V_D + (0 \text{ A})R$$

$$V_D = E\big|_{I_D=0 \text{ A}}$$ (2.3)

as shown in Fig. 2.2. A straight line drawn between the two points will define the load line as depicted in Fig. 2.2. Change the level of R (the load) and the intersection on the vertical axis will change. The result will be a change in the slope of the load line and a different point of intersection between the load line and the device characteristics. We now have a load line defined by the network and a characteristic curve defined by the device. The point of intersection between the two is the point of operation for this circuit. By simply drawing a line down to the horizontal axis the diode voltage V_{DQ} can be determined, whereas a horizontal line from the point of intersection to the vertical axis will provide the level of I_{DQ}. The current I_D is actually the current through the entire series configuration of Fig. 2.1. The point of operation is usually called the quiescent point (abbreviated "Q-pt.") to reflect its "still, unmoving" qualities as defined by a dc network.

The solution obtained at the intersection of the two curves is the same that would be obtained by a simultaneous mathematical solution of Eqs. (2.1) and (1.4) [$I_D = Is(e^{kVD/TK}$ _ 1)]. Since the curve for a diode has nonlinear characteristics the mathematics involved would require the use of nonlinear techniques that are beyond the needs and scope of this book. The load-line analysis described above provides a solution with a minimum of effort and a "pictorial" description of why the levels of solution for V_{DQ} and I_{DQ} were obtained. The next two examples will demonstrate the techniques introduced above and reveal the relative ease with which the load line can be drawn using Eqs. (2.2) and (2.3).
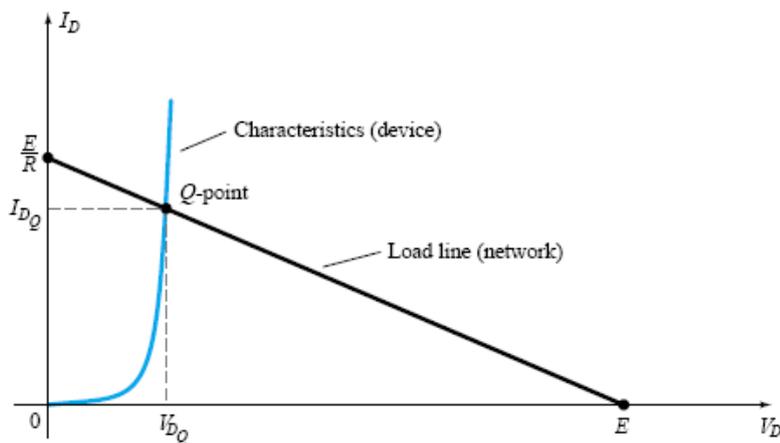

Figure 2.2 Drawing the load line and finding the point of operation.

EXAMPLE 2.1: For the series diode configuration of Fig. 2.3a employing the diode characteristics of
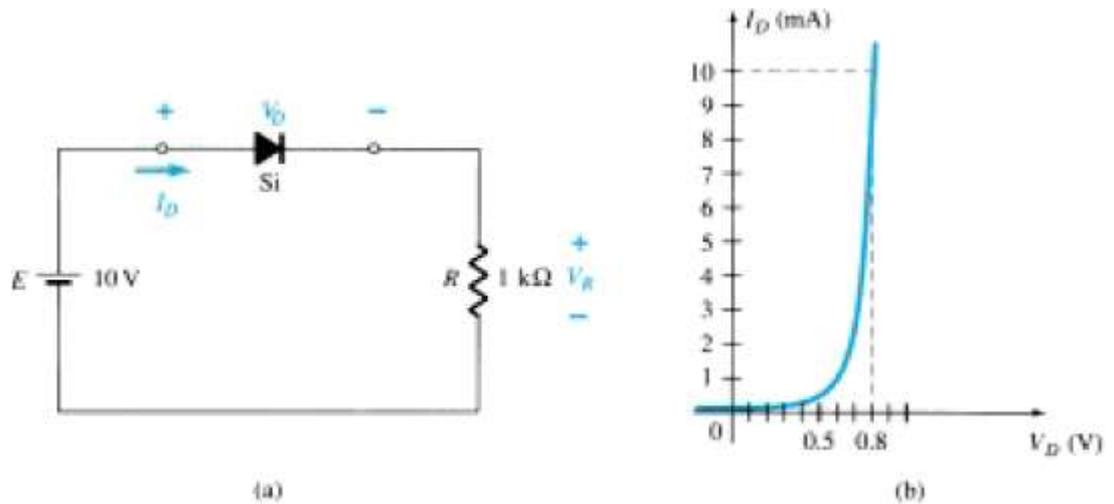Fig. 2.3b determine:
(a) V_{DQ} and I_{DQ}.
(b) V_R.

(a)   (b)

Figure 2.3 (a) Circuit; (b) characteristics.

(a) Eq. (2.2): $I_D = \dfrac{E}{R}\Big|_{V_D=0\,V} = \dfrac{10\ V}{2\ k\Omega} = 10\ mA$

Eq. (2.3): $V_D = E|_{I_D=0\,A} = 10\ V$

The resulting load line appears in Fig. 2.4. The intersection between the load line and the characteristic curve defines the Q-point as

$V_{D_Q} \cong 0.78\ V$

$I_{D_Q} \cong 9.25\ mA$

The level of V_D is certainly an estimate, and the accuracy of I_D is limited by the chosen scale. A higher degree of accuracy would require a plot that would be much larger and perhaps unwieldy.

(b) $V_R = I_R R = I_{D_Q} R = (9.25\ mA)(1\ k\Omega) = 9.25\ V$

or $V_R = E - V_D = 10\ V - 0.78\ V = 9.22\ V$

The difference in results is due to the accuracy with which the graph can be read. Ideally, the results obtained either way should be the same.
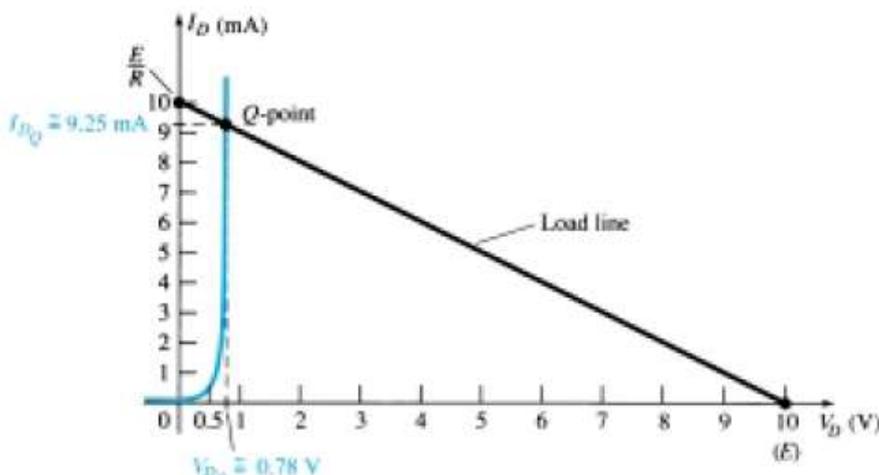
Figure 2.4 Solution to Example 2.1

SINUSOIDAL INPUTS; HALF-WAVE RECTIFICATION :-

The simplest of networks to examine with a time-varying signal appears in Fig. 2.43. For the moment we will use the ideal model (note the absence of the Si or Ge label to denote ideal diode) to ensure that the approach is not clouded by additional mathematical complexity.
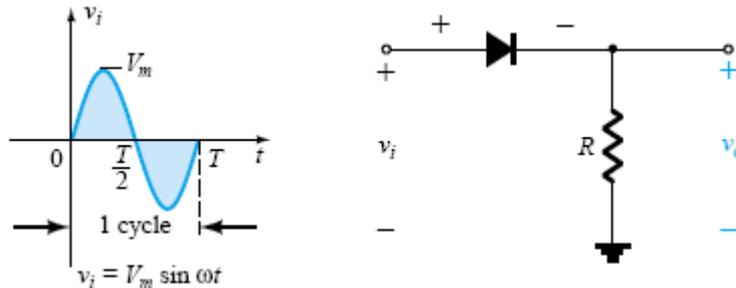

Figure 2.43 Half-wave rectifier.

Over one full cycle, defined by the period T of Fig. 2.43, the average value (the algebraic sum of the areas above and below the axis) is zero. The circuit of Fig. 2.43, called a half-wave rectifier, will generate a waveform vo that will have an average value of particular, use in the ac-to-dc conversion process. When employed in the rectification process, a diode is typically referred to as a rectifier. Its power and current ratings are typically much higher than those of diodes employed in other applications, such as computers and communication systems. During the interval t = 0 → T/2 in Fig. 2.43 the polarity of the applied voltage vi is such as to establish "pressure" in the direction indicated and turn on the diode with the polarity appearing above the diode. Substituting the short-circuit equivalence for the ideal diode will result in the equivalent circuit of Fig. 2.44, where it is fairly obvious that the output signal is an exact replica of the applied signal. The two terminals defining the output voltage are connected directly to the applied signal via the short-circuit equivalence of the diode.
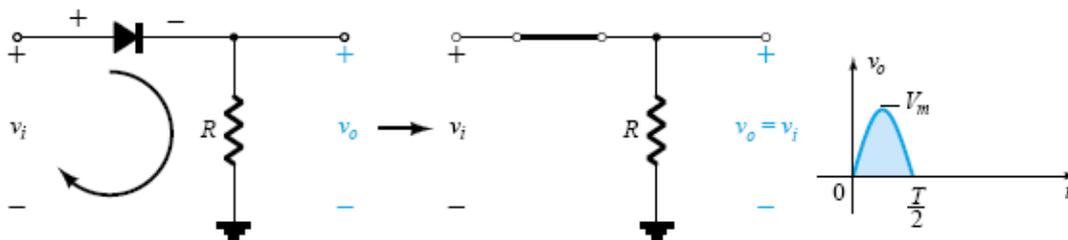

Figure 2.44 Conduction region (0 → T/2).

For the period T/2 → T, the polarity of the input vi is as shown in Fig. 2.45 and the resulting polarity across the ideal diode produces an "off" state with an open-circuit equivalent. The result is the absence of a path for charge to flow and vo= iR =(0)R = 0 V for the period T/2 → T. The input vi and the output vo were sketched together in Fig. 2.46 for comparison purposes. The output signal vo now has a net positivearea above the axis over a full period and an average value determined by:

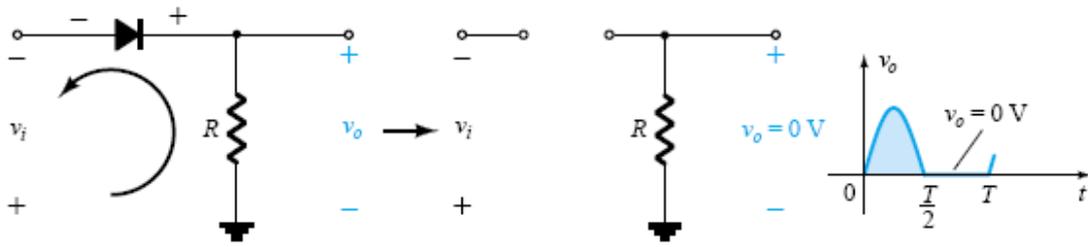$$V_{dc} = 0.318V_m \quad \text{half-wave} \quad (2.7)$$

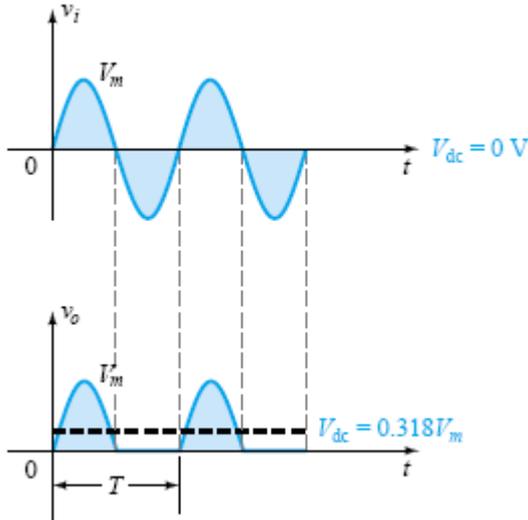**Figure 2.45** Nonconduction region (T/2 →T).

Figure 2.46 Half-wave rectified signal.

The process of removing one-half the input signal to establish a dc level is aptly called half-wave rectification. The effect of using a silicon diode with V_T = 0.7 V is demonstrated in Fig. 2.47 for the forward-bias region. The applied signal must now be at least 0.7 V before the diode can turn "on." For levels of vi less than 0.7 V, the diode is still in an opencircuit state and vo = 0 V as shown in the same figure. When conducting, the difference between vo and vi is a fixed level of V_T = 0.7 V and vo = vi _ V_T, as shown in the figure. The net effect is a reduction in area above the axis, which naturally reduces the resulting dc voltage level. For situations where Vm >>V_T, Eq. 2.8 can be applied to determine the average value with a relatively high level of accuracy.

$$V_{dc} \cong 0.318(V_m - V_T)$$ (2.8)

In fact, if Vm is sufficiently greater than V_T, Eq. 2.7 is often applied as a first approximation for V_{dc}.
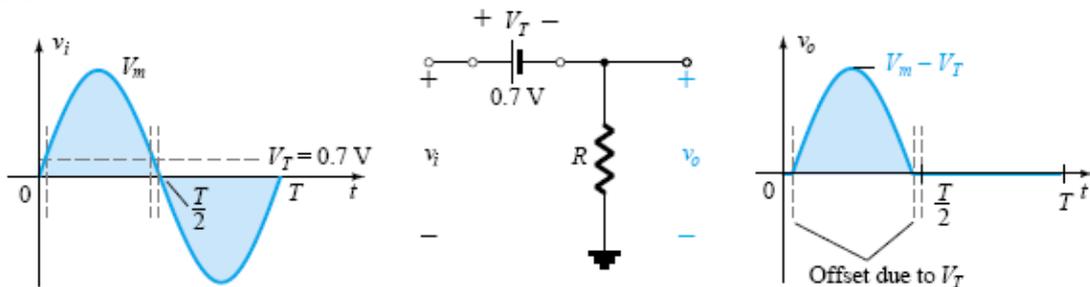
Figure 2.47 Effect of V_T on half-wave rectified signal.

PIV (PRV) :-

The peak inverse voltage (PIV) [or PRV (peak reverse voltage)] rating of the diode is of primary importance in the design of rectification systems. Recall that it is the voltage rating that must not be exceeded in the reverse-bias region or the diode will enter the Zener avalanche region. The required PIV rating for the half-wave rectifier can be determined from Fig. 2.51, which displays the reverse-biased diode of Fig. 2.43 with maximum applied voltage. Applying Kirchhoff"s voltage law, it is fairly obvious that the PIV rating of the diode must equal or exceed the peak value of the applied voltage. Therefore,

$$\boxed{\text{PIV rating} \geq V_m} \quad \text{half-wave rectifier} \qquad (2.9)$$
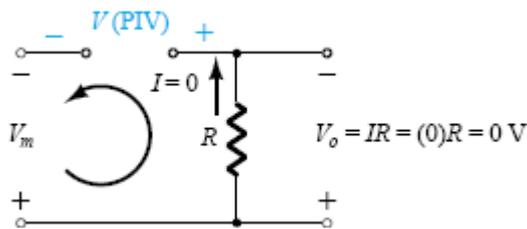
Figure 2.51 Determining the required PIV rating for the halfwave rectifier.

FULL-WAVE RECTIFICATION :-

1- Bridge Network :-

The dc level obtained from a sinusoidal input can be improved 100% using a process called full-wave rectification. The most familiar network for performing such a function appears in Fig. 2.52 with its four diodes in a bridge configuration. During the period t = 0 to T/2 the polarity of the input is as shown in Fig. 2.53. The resulting polarities across the ideal diodes are also shown in Fig. 2.53 to reveal that D2 and D3 are conducting while D1 and D4 are in the "off" state. The net result is the configuration of Fig. 2.54, with its indicated current and polarity across R. Since the diodes are ideal the load voltage is vo = vi, as shown in the same figure.
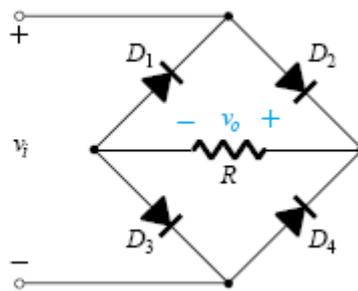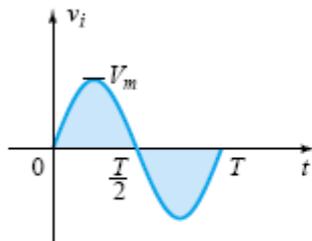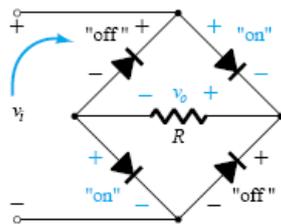

Figure 2.52 Full-wave bridge rectifier.

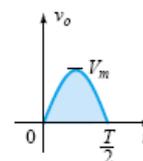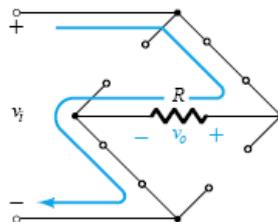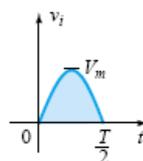Figure 2.53 Network of Fig. 2.52 for the period 0 → T/2 of the input voltage v_i.

Figure 2.54 Conduction path for the positive region of v_i.

For the negative region of the input the conducting diodes are D1 and D4, resulting in the configuration of Fig. 2.55. The important result is that the polarity across the load resistor R is the same as in Fig. 2.53, establishing a second positive pulse, as shown in Fig. 2.55. Over one full cycle the input and output voltages will appear as shown in Fig. 2.56.
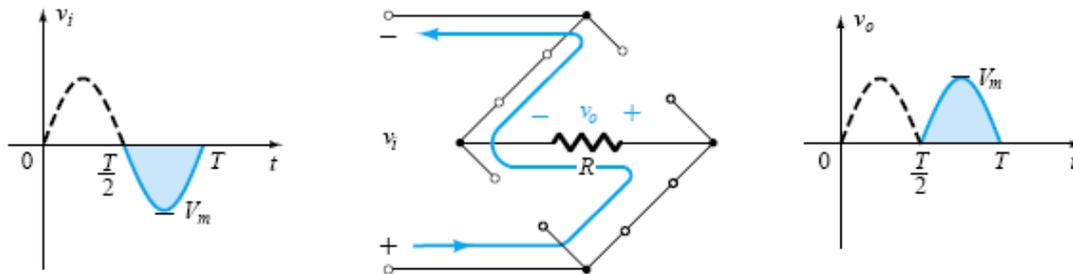

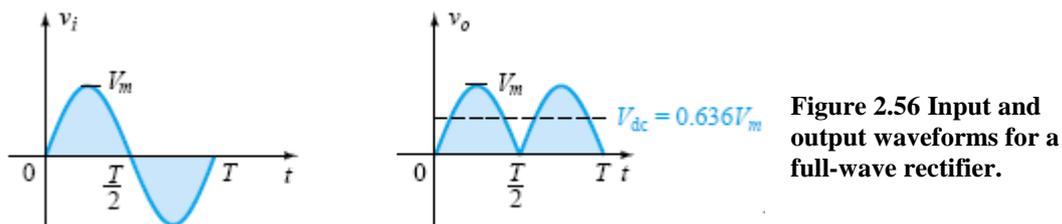**Figure 2.55 Conduction path for the negative region of vi.**

Figure 2.56 Input and output waveforms for a full-wave rectifier.

Since the area above the axis for one full cycle is now twice that obtained for a half-wave system, the dc level has also been doubled and

$$V_{dc} = 2(\text{Eq. } 2.7) = 2(0.318V_m)$$

$$\boxed{V_{dc} = 0.636V_m} \quad \text{full-wave} \qquad\qquad (2.10)$$

If silicon rather than ideal diodes are employed as shown in Fig. 2.57, an application of Kirchhoff's voltage law around the conduction path would result in

$$v_i - V_T - v_o - V_T = 0$$

$$v_o = v_i - 2V_T$$

The peak value of the output voltage vo is therefore

$$V_{o_{max}} = V_m - 2V_T$$

For situations where Vm >>2VT, Eq. (2.11) can be applied for the average value with a relatively high level of accuracy.
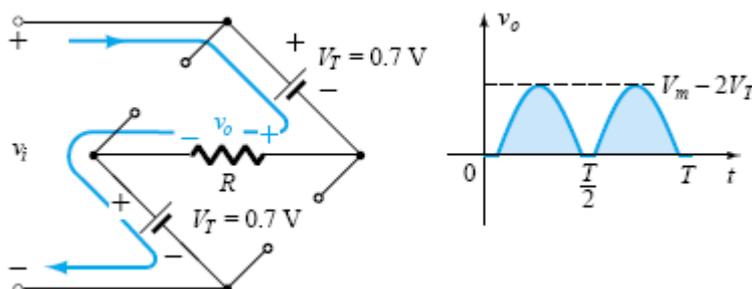
$$\boxed{V_{dc} \cong 0.636(V_m - 2V_T)} \qquad\qquad (2.11)$$

Figure 2.57 Determining Vomax for silicon diodes in the bridge configuration.

Then again, if **Vm** is sufficiently greater than **2VT**, then Eq. (2.10) is often applied as a first approximation for **Vdc**. The required PIV of each diode (ideal) can be determined from Fig. 2.58 obtained at the peak of the positive region of the input signal. For the indicated loop the maximum voltage across R is Vm and the PIV rating is defined by

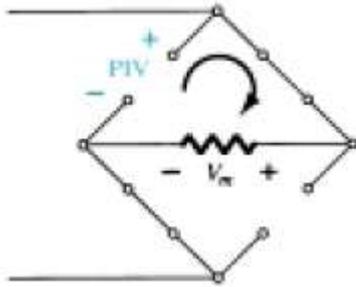$$PIV \cong V_m \qquad \text{full-wave bridge rectifier} \qquad (2.12)$$

Figure 2.58 Determining the required PIV for the bridge configuration.

Center-Tapped Transformer:-

A second popular full-wave rectifier appears in Fig. 2.59 with only two diodes but requiring a center-tapped (CT) transformer to establish the input signal across each section of the secondary of the transformer. During the positive portion of vi applied to the primary of the transformer, the network will appear as shown in Fig. 2.60. D1 assumes the short-circuit equivalent and D2 the open-circuit equivalent, as determined by the secondary voltages and the resulting current directions. The output voltage appears as shown in Fig. 2.60.
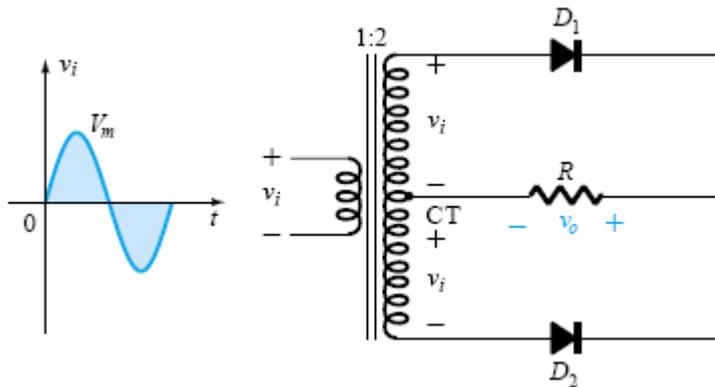

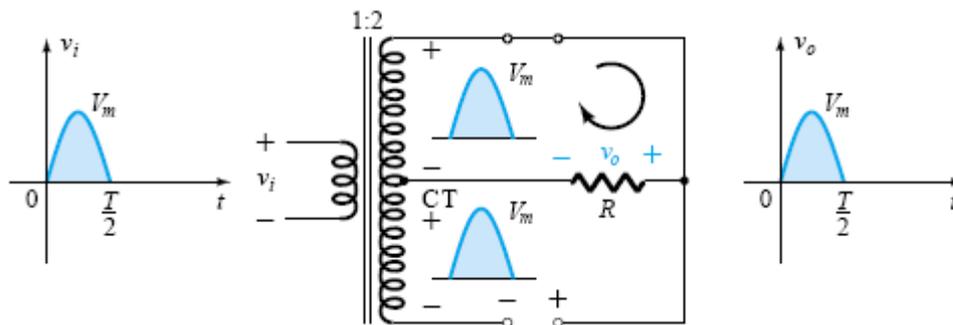**Figure 2.59 Center-tapped transformer full-wave rectifier.**

Figure 2.60 Network conditions for the positive region of vi.

During the negative portion of the input the network appears as shown in Fig2.61, reversing the roles of the diodes but maintaining the same polarity for

the voltage across the load resistor R. The net effect is the same output as that appearing in Fig. 2.56 with the same dc levels. The network of Fig. 2.62 will help us determine the net PIV for each diode for this full-wave rectifier. Inserting the maximum voltage for the secondary voltage and Vm as established by the adjoining loop will result in

$$PIV = V_{secondary} + V_R$$

$$= V_m + V_m$$

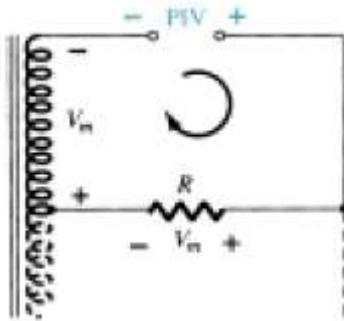$$\boxed{PIV \geq 2V_m} \quad \text{CT transformer, full-wave rectifier} \qquad (2.13)$$

Figure 2.62 Determining the PIV level for the diodes of the CT transformer full-wave rectifier.

CLIPPERS :-

There are a variety of diode networks called clippers that have the ability to "clip" off a portion of the input signal without distorting the remaining part of the alternating waveform. The half-wave rectifier of Section 2.7 is an example of the simplest form of diode clipper—one resistor and diode. Depending on the orientation of the diode, the positive or negative region of the input signal is "clipped" off. There are two general categories of clippers: series and parallel. The series configuration is defined as one where the diode is in series with the load, while the parallel variety has the diode in a branch parallel to the load.

1- Series clipper

The response of the series configuration of Fig. 2.67a to a variety of alternating waveforms is provided in Fig. 2.67b. Although first introduced as a half-wave rectifier (for sinusoidal waveforms), there are no boundaries on the type of signals that can be applied to a clipper. The addition of a dc supply such as shown in Fig. 2.68 can have a pronounced effect on the output of a clipper. Our initial discussion will be limited to ideal diodes, with the effect of VT reserved for a concluding example.
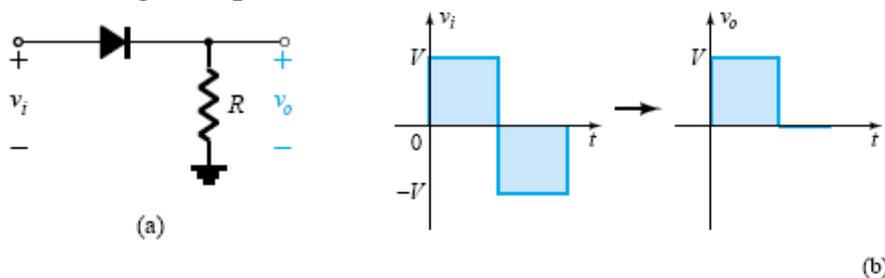

Figure 2.67 Series clipper.

For the network of Fig. 2.68, the direction of the diode suggests that the signal vi must be positive to turn it on. The dc supply further requires that the voltage vi be greater than V volts to turn the diode on. The negative region of the input signal is

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"pressuring" the diode into the "off" state, supported further by the dc supply. In general, therefore, we can be quite sure that the diode is an open circuit ("off" state) for the negative region of the input signal. For the ideal diode the transition between states will occur at the point on the characteristics where vd = 0 V and id = 0 A. Applying the condition id = 0 at vd = 0 to the network of Fig. 2.68 will result in the configuration of Fig. 2.69, where it is recognized that the level of vi that will cause a transition in state is
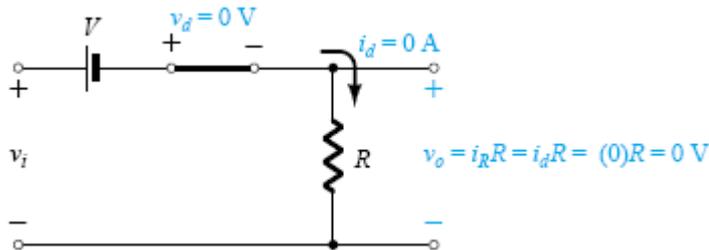
$$v_i = V \qquad\qquad (2.14)$$

Figure 2.69 Determining the transition level for the circuit of Fig. 2.68.

For an input voltage greater than V volts the diode is in the short-circuit state, while for input voltages less than V volts it is in the open-circuit or "off" state. When the diode is in the short-circuit state, such as shown in Fig. 2.70, the output voltage vo can be determined by applying Kirchhoff's voltage law in the clockwise direction:

$$v_i - V - v_o = 0 \text{ (CW direction)}$$

$$v_o = v_i - V \qquad\qquad (2.15)$$

It is then possible that the output voltage can be sketched from the resulting data points of vo as demonstrated in Fig. 2.71. Keep in mind that at an instantaneous value of vi the input can be treated as a dc supply of that value and the corresponding dc value (the instantaneous value) of the output determined. For instance, at vi =Vm for the network of Fig. 2.68, the network to be analyzed appears in Fig. 2.72. For Vm > V the diode is in the short-circuit state and vo = Vm =V, as shown in Fig. 2.71. At vi _ V the diodes change state; at vi =–Vm, vo = 0 V; and the complete curve for vo can be sketched as shown in Fig. 2.73.
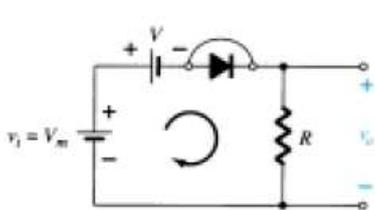

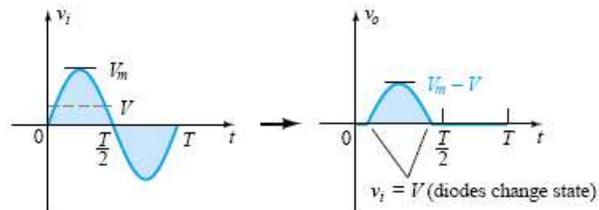Figure 2.72 Determining v_o when $v_i = V_m$.

Figure 2.73 Sketching v_o.

Parallel clipper:-

The network of Fig. 2.82 is the simplest of parallel diode configurations with the output for the same inputs of Fig. 2.67. The analysis of parallel configurations is very similar to that applied to series configurations, as demonstrated in the next example.
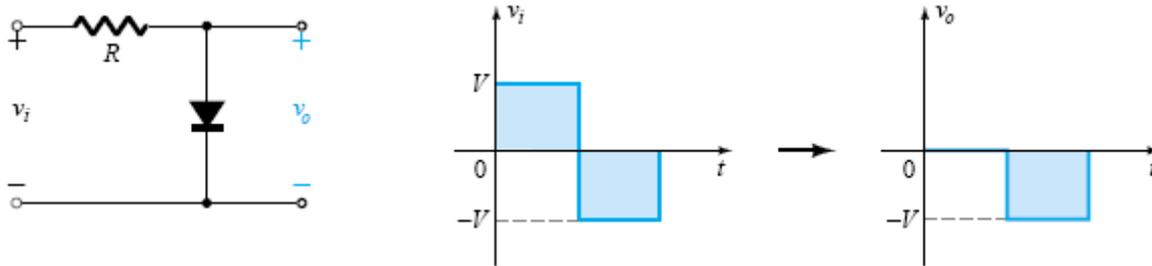
Figure 2.82 Response to a parallel clipper.

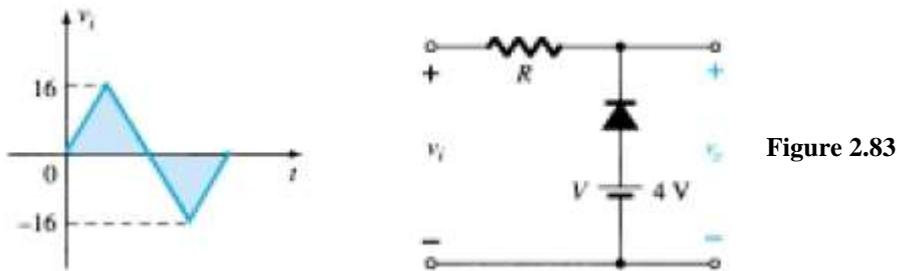## EXAMPLE :- Determine vo for the network of Fig. 2.83.

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Figure 2.83

Solution

The polarity of the dc supply and the direction of the diode strongly suggest that the diode will be in the "on" state for the negative region of the input signal. For this region the network will appear as shown in Fig. 2.84, where the defined terminals for vo require that vo =V =4 V.

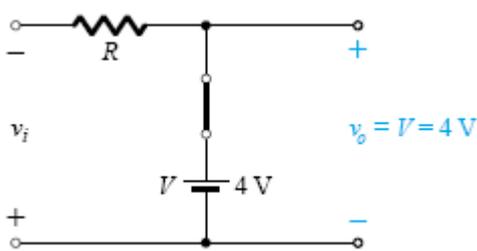**Figure 2.84 vo for the negative region of vi.**

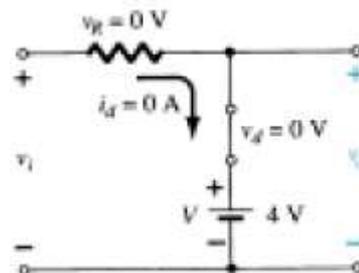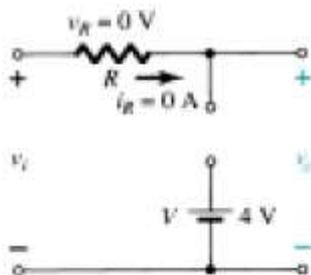**Figure 2.85 Determining the transition level .**

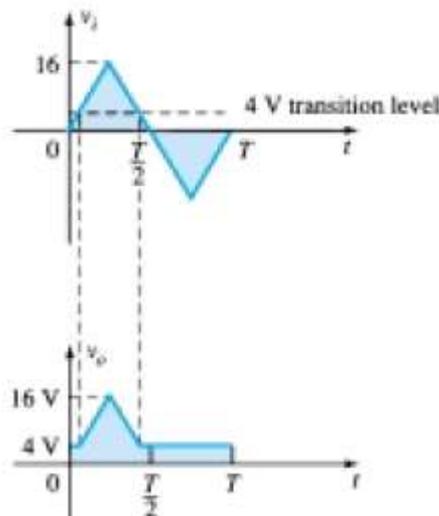**Figure 2.86** Determining v_o for the open state of the diode.

Figure 2.87 Sketching vo

The transition state can be determined from Fig. 2.85, where the condition id _ 0 A at vd =0 V has been imposed. The result is vi (transition) = V = 4 V.
Since the dc supply is obviously "pressuring" the diode to stay in the shortcircuit state, the input voltage must be greater than 4 V for the diode to be in the "off" state. Any input voltage less than 4 V will result in a short-circuited diode.
For the open-circuit state the network will appear as shown in Fig. 2.86, where vo =vi. Completing the sketch of vo results in the waveform of Fig. 2.87.

CLAMPERS :-
The clamping network is one that will "clamp" a signal to a different dc level. The network must have a capacitor, a diode, and a resistive element, but it can also employ an independent dc supply to introduce an additional shift. The magnitude of R and C must be chosen such that the time constant _ RC is large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is nonconducting. Throughout the analysis we will assume that for all practical purposes the capacitor will fully charge or discharge in five time constants. The network of Fig. 2.92 will clamp the input signal to the zero level (for ideal diodes). The resistor R can be the load resistor or a parallel combination of the load resistor and a resistor designed to provide the desired level of R.
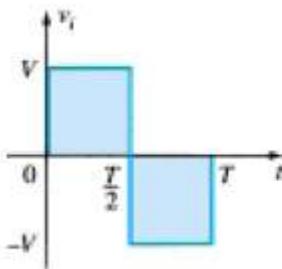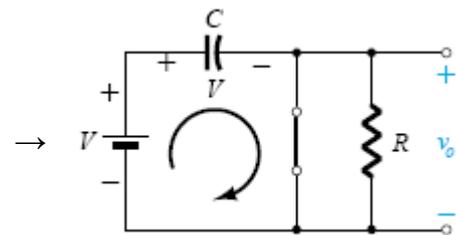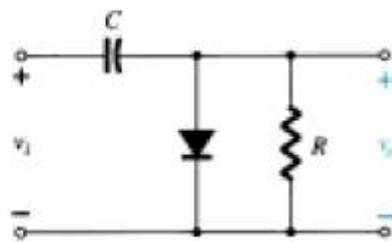

Figure 2.92 Clamper.

Figure 2.93 Diode "on" and the capacitor charging to V volts

During the interval 0 →T/2 the network will appear as shown in Fig. 2.93, with the diode in the "on" state effectively "shorting out" the effect of the resistor R. The resulting RC time constant is so small (R determined by the inherent resistance of the network) that the capacitor will charge to V volts very quickly. During this interval the output voltage is directly across the short circuit and vo = 0 V.
When the input switches to the –V state, the network will appear as shown in Fig. 2.94, with the open-circuit equivalent for the diode determined by the applied signal and stored voltage across the capacitor—both "pressuring" current through the diode from cathode to anode. Now that R is back in the network the time constant determined by the RC product is sufficiently large to establish a discharge period 5 much greater than the period T/2 □ T, and it can be assumed on an approximate basis that the capacitor holds onto all its charge and, therefore, voltage (since V =Q/C) during this period. Since vo is in parallel with the diode and resistor, it can also be drawn in the alternative position shown in Fig. 2.94. Applying Kirchhoff's voltage law around the input loop will result in

$$-V - V - v_o = 0$$
$$v_o = -2V$$

The negative sign resulting from the fact that the polarity of 2V is opposite to the polarity defined for vo. The resulting output waveform appears in Fig. 2.95 with the input signal. The output signal is clamped to 0 V for the interval 0 to T/2 but maintains the same total swing (2V) as the input. For a clamping network: The total swing of the output is equal to the total swing of the input signal. This fact is an excellent checking tool for the result obtained.In general, the following steps may be helpful when analyzing clamping networks:

1. Start the analysis of clamping networks by considering that part of the input signal that will forward bias the diode.
The statement above may require skipping an interval of the input signal (as demonstrated in an example to follow), but the analysis will not be extended by an unnecessary measure of investigation.

2. During the period that the diode is in the "on" state, assume that the capacitor will charge up instantaneously to a voltage level determined by the network.

3. Assume that during the period when the diode is in the "off" state the capacitor will hold on to its established voltage level.

4. Throughout the analysis maintain a continual awareness of the location and reference polarity for vo to ensure that the proper levels for vo are obtained.

5. Keep in mind the general rule that the total swing of the total output must match the swing of the input signal.
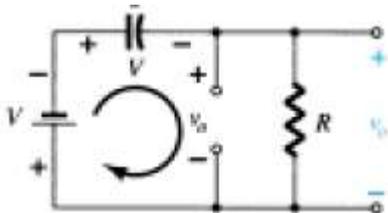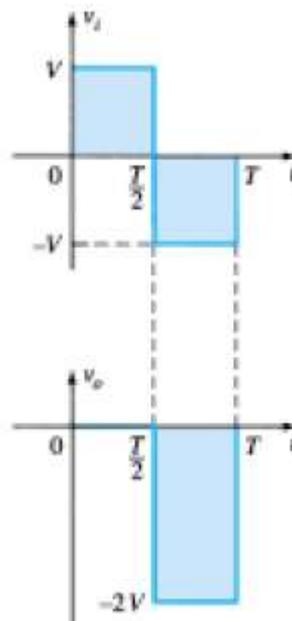

Figure 2.94 Determining vo with the diode "off."

Figure 2.95 Sketching vo for the network of Fig. 2.92.

A number of clamping circuits and their effect on the input signal are shown in Fig. 2.103. Although all the waveforms appearing in Fig. 2.103 are square waves, clamping networks work equally well for sinusoidal signals. In fact, one approach to the analysis of clamping networks with sinusoidal inputs is to replace the sinusoidal signal by a square wave of the same peak values. The resulting output will then form an envelope for the sinusoidal response as shown in Fig. 2.104 for a network appearing in the bottom right of Fig. 2.103.
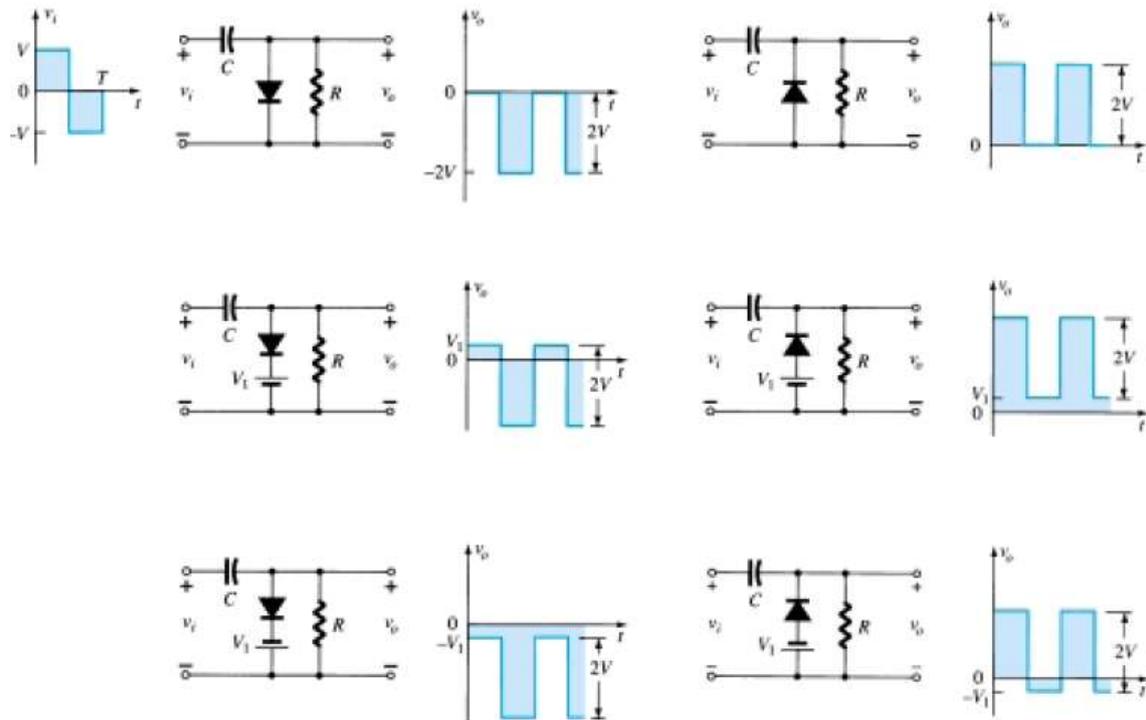

Figure 2.103 Clamping circuits with ideal diodes (5 = 5RC >> T/2).

ZENER DIODES:-

The analysis of networks employing Zener diodes is quite similar to that applied to the analysis of semiconductor diodes in previous sections. First the state of the diode must be determined followed by a substitution of the appropriate model and a determination of the other unknown quantities of the network.

The simplest of Zener diode networks appears in Fig. 2.106. The applied dc voltage is fixed, as is the load resistor. The analysis can fundamentally be broken down into two steps.

 1. Determine the state of the Zener diode by removing it from the network and calculating the voltage across the resulting open circuit. Applying step 1 to the network of Fig. 2.106 will result in the network of Fig. 2.107, where an application of the voltage divider rule will result in

$$V = V_L = \frac{R_L V_i}{R + R_L}$$

If $V \geq V_Z$, the Zener diode is "on" and the equivalent model of Fig. 2.105a can be substituted. If $V < V_Z$, the diode is "off" and the open-circuit equivalence of Fig. 2.105b is substituted.

2. Substitute the appropriate equivalent circuit and solve for the desired unknowns. For the network of Fig. 2.106, the "on" state will result in the equivalent network of Fig. 2.108. Since voltages across parallel elements must be the same, we find that
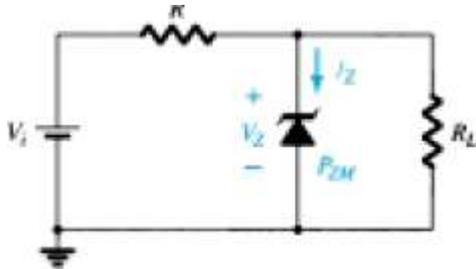
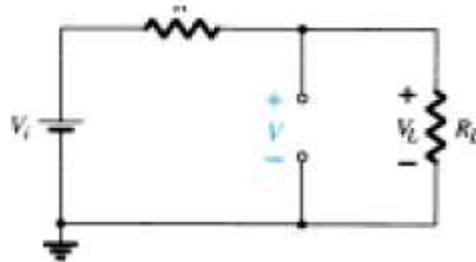$$V_L = V_Z$$

Figure 2.106 Basic Zener regulator   **Figure 2.107 Determining the**
                                                  state of the Zener diode.

The Zener diode current must be determined by an application of Kirchhoff's current law. That is,

$$I_R = I_Z + I_L$$

$$I_Z = I_R - I_L \qquad\qquad (2.18)$$

$$I_L = \frac{V_L}{R_L} \quad and \quad I_R = \frac{V_R}{R} = \frac{V_i - V_L}{R}$$

The power dissipated by the Zener diode is determined by

$$P_Z = V_Z I_Z$$

which must be less than the PZM specified for the device.

Before continuing, it is particularly important to realize that the first step was employed only to determine the state of the Zener diode. If the Zener diode is in the "on" state, the voltage across the diode is not V volts. When the system is turned on, the Zener diode will turn "on" as soon as the voltage across the Zener diode is VZ volts. It will then "lock in" at this level and never reach the higher level of V volts. Zener diodes are most frequently used in regulator networks or as a reference voltage. Figure 2.106 is a simple regulator designed to maintain a fixed voltage across the load RL. For values of applied voltage greater than required to turn the Zener diode "on," the voltage across the load will be maintained at VZ volts. If the Zener diode is employed as a reference voltage, it will provide a level for comparison against other voltages.

Fixed Vi, Variable RL :-

Due to the offset voltage VZ, there is a specific range of resistor values (and therefore load current) which will ensure that the Zener is in the "on" state. Too small a load resistance RL will result in a voltage VL across the load resistor less than VZ , and the

Zener device will be in the "off" state. To determine the minimum load resistance , that will turn the Zener diode on, simply calculate the value of R_L that will result in a load voltage $V_L = V_Z$. That is,

$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

Solving for RL, we have

$$\boxed{R_{L_{min}} = \frac{R V_Z}{V_i - V_Z}}$$

Any load resistance value greater than the R_L obtained from Eq. (2.20) will ensure that the Zener diode is in the "on" state and the diode can be replaced by its V_Z source equivalent. The condition defined by Eq. (2.20) establishes the minimum RL but in turn specifies the maximum I_L as

$$\boxed{I_{L_{max}} = \frac{V_L}{R_L} = \frac{V_Z}{R_{L_{min}}}}$$

Once the diode is in the "on" state, the voltage across R remains fixed at

$$\boxed{V_R = V_i - V_Z}$$

and IR remains fixed at

$$\boxed{I_R = \frac{V_R}{R}}$$

The Zener current $\qquad \boxed{I_Z = I_R - I_L}$

resulting in a minimum I_Z when I_L is a maximum and a maximum I_Z when I_L is a minimum value since I_R is constant. Since I_Z is limited to I_{ZM} as provided on the data sheet, it does affect the range of R_L and therefore I_L. Substituting I_{ZM} for I_Z establishes the minimum I_L as

$$\boxed{I_{L_{min}} = I_R - I_{ZM}}$$

and the maximum load resistance as

$$\boxed{R_{L_{max}} = \frac{V_Z}{I_{L_{min}}}}$$

Fixed RL, Variable Vi :-
For fixed values of R_L in Fig. 2.106, the voltage Vi must be sufficiently large to turn the Zener diode on. The minimum turn-on voltage Vi = Vimin is determined by

$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

$$\boxed{V_{i_{min}} = \frac{(R_L + R)V_Z}{R_L}}$$

The maximum value of Vi is limited by the maximum Zener current I_{ZM}. Since $I_{ZM} = I_R - I_L$,

$$\boxed{I_{R_{max}} = I_{ZM} + I_L}$$

Since I_L is fixed at V_Z/R_L and I_{ZM} is the maximum value of I_Z, the maximum Vi is defined by

$$V_{i_{max}} = V_{R_{max}} + V_Z$$

$$\boxed{V_{i_{max}} = I_{R_{max}}R + V_Z}$$

Voltage Doubler :-

The network of Figure 2.121 is a half-wave voltage doubler. During the positive voltage half-cycle across the transformer, secondary diode D_1 conducts (and diode D_2 is cut off), charging capacitor C_1 up to the peak rectified voltage (Vm). Diode $_{D1}$ is ideally a short during this half-cycle, and the input voltage charges capacitor C_1 to Vm with the polarity shown in Fig. 2.122a. During the negative half-cycle of the secondary voltage, diode D_1 is cut off and diode D_2 conducts charging capacitor C_2. Since diode D_2 acts as a short during the negative half-cycle (and diode D1 is open), we can sum the voltages around the outside loop

$$-V_m - V_{C_1} + V_{C_2} = 0$$
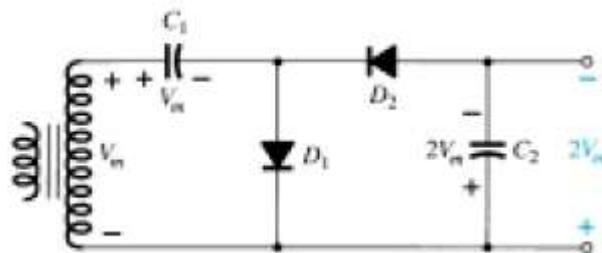$$-V_m - V_m + V_{C_2} = 0$$

$$V_{C_2} = 2V_m$$

Figure 2.121 Half-wave voltage doubler.

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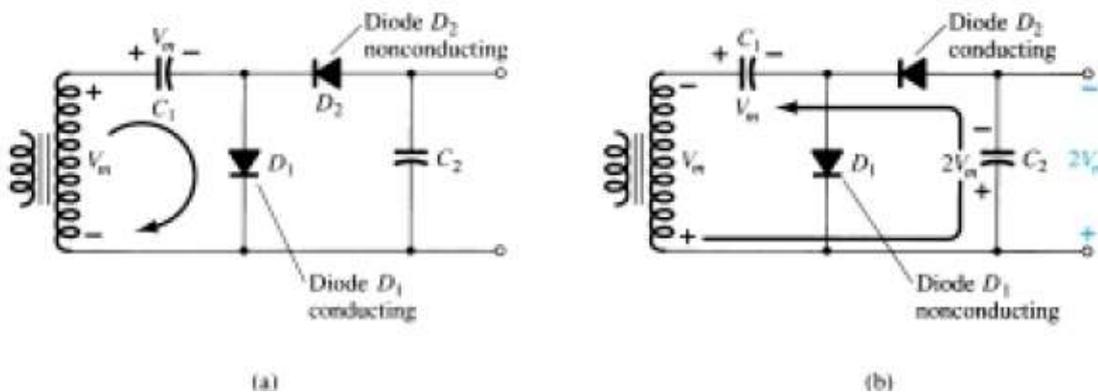(a)   (b)

Figure 2.122 Double operation, showing each half-cycle of operation: (a) positive half-cycle; (b) negative half cycle.

On the next positive half-cycle, diode D2 is nonconducting and capacitor C2 will discharge through the load. If no load is connected across capacitor C2, both

capacitors stay charged—C_1 to Vm and C_2 to 2Vm. If, as would be expected, there is a load connected to the output of the voltage doubler, the voltage across capacitor C_2 drops during the positive half-cycle (at the input) and the capacitor is recharged up to 2Vm during the negative half-cycle. The output waveform across capacitor C_2 is that of a half-wave signal filtered by a capacitor filter. The peak inverse voltage across each diode is 2Vm.

Another doubler circuit is the full-wave doubler of Fig. 2.123. During the positive half-cycle of transformer secondary voltage (see Fig. 2.124a) diode D_1 conducts charging capacitor C_1 to a peak voltage Vm. Diode D_2 is nonconducting at this time
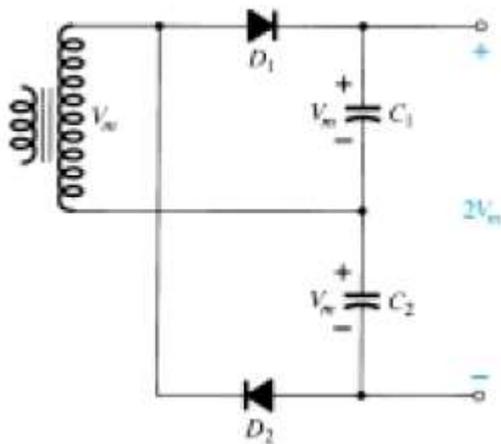

Figure 2.123 Full-wave voltage doubler.
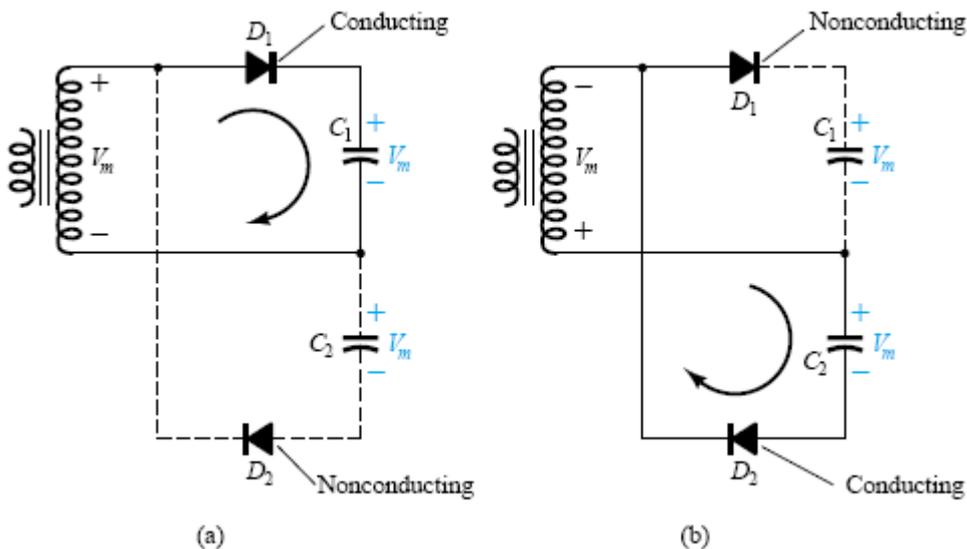

(a)   (b)

Figure 2.124 Alternate halfcycles of operation for full-wave voltage doubler.

During the negative half-cycle (see Fig. 2.124b) diode D_2 conducts charging capacitor C_2 while diode D_1 is nonconducting. If no load current is drawn from the circuit, the voltage across capacitors C_1 and C_2 is 2Vm. If load current is

drawn from the circuit, the voltage across capacitors C_1 and C_2 is the same as that across a capacitor fed by a full-wave rectifier circuit. One difference is that the effective capacitance is that of C_1 and C_2 in series, which is less than the capacitance of either C_1 or C_2 alone. The lower capacitor value will provide poorer filtering action than the singlecapacitor filter circuit. The peak inverse voltage across each diode is 2Vm, as it is for the filter capacitor circuit. In summary, the half-wave or full-wave voltage-doubler circuits provide twice the peak voltage of the transformer secondary while requiring no center-tapped transformer and only 2Vm PIV rating for the diodes.
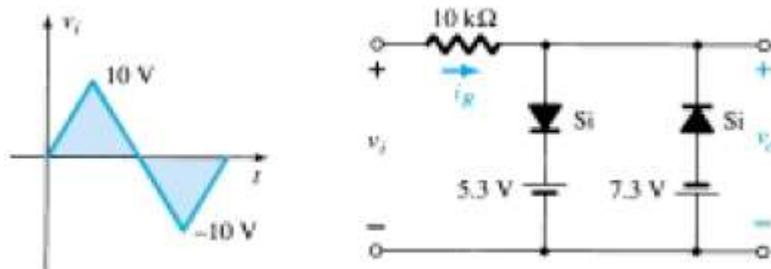
Questions:-

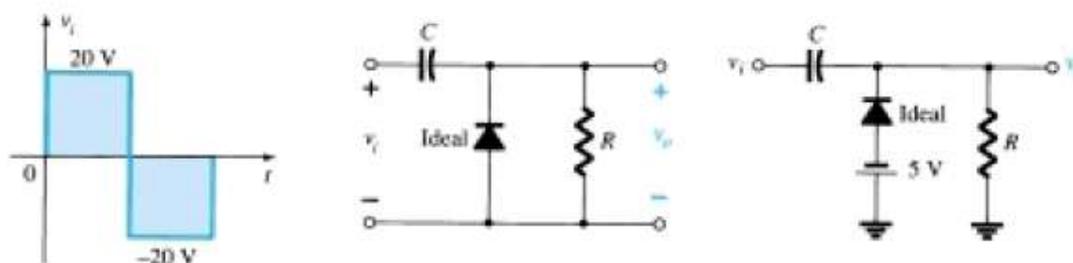**1-Determine vo for each network for the input shown.**
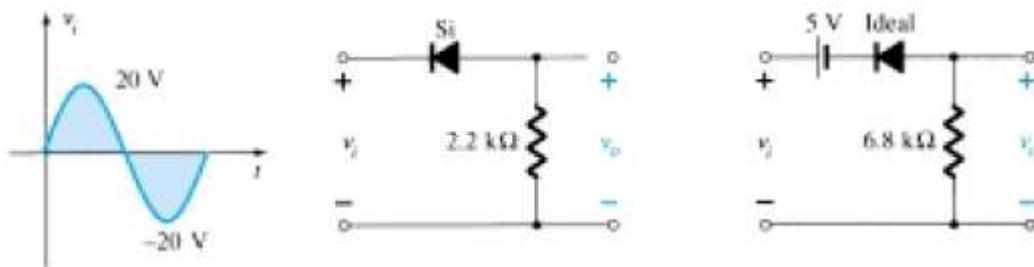
2- Determine vo for each network for the input shown.
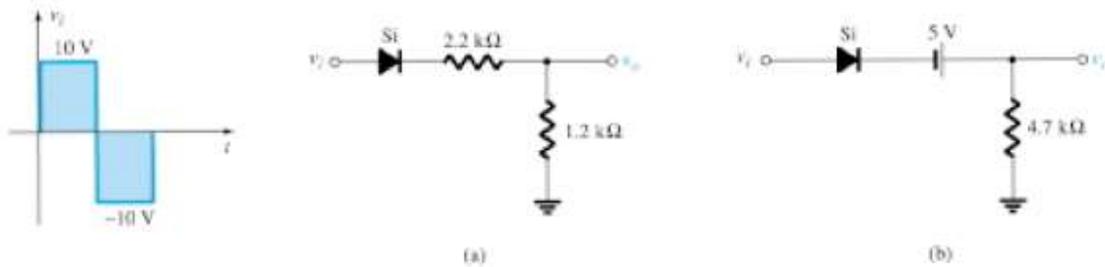
3- Sketch iR and vo for the network for the input shown.

4-Sketch vo for each network of Fig. 2.160 for the input shown.

Bipolar JunctionTransistors:-

The transistor is a three-layer semiconductor device consisting of either two n- and one p-type layers of material or two p- and one n-type layers of material. The former is called an npn transistor, while the latter is called a pnp transistor. Both are shown in Fig. 3.2 with the proper dc biasing. We will find in Chapter 4 that the dc biasing is necessary to establish the proper region of operation for ac amplification. The emitter layer is heavily doped, the base lightly doped, and the collector only lightly doped. The outer layers have widths much greater than the sandwiched p- or n-type material. For the transistors shown in Fig. 3.2 the ratio of the total width to that of the center layer is 0.150/0.001 _ 150_1. The doping of the sandwiched layer is also considerably less than that of the outer layers (typically, 10_1 or less). This lower doping level decreases the conductivity (increases the resistance) of this material by limiting the number of "free" carriers.

For the biasing shown in Fig. 3.2 the terminals have been indicated by the capital letters E for emitter, C for collector, and B for base. An appreciation for this choice of notation will develop when we discuss the basic operation of the transistor. The abbreviation BJT, from bipolar junction transistor, is often applied to this threeterminal device. The term bipolar reflects the fact that holes and electrons participate in the injection process into the oppositely polarized material. If only one carrier is employed (electron or hole), it is considered a unipolar device. The Schottky diode of Chapter 20 is such a device.
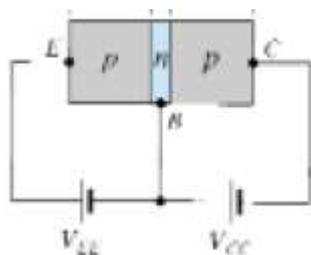

Figure 3.2 Type of transistors:

TRANSISTOR OPERATION :-

The basic operation of the transistor will now be described using the pnp transistor of Fig. 3.2a. The operation of the npn transistor is exactly the same if the roles played by the electron and hole are interchanged. In Fig. 3.3 the pnp transistor has been redrawn without the base-to-collector bias. Note the similarities between this situation and that of the forward-biased diode in Chapter 1. The depletion region has been reduced in width due to the applied bias, resulting in a heavy flow of majority carriers from the p- to the n-type material.
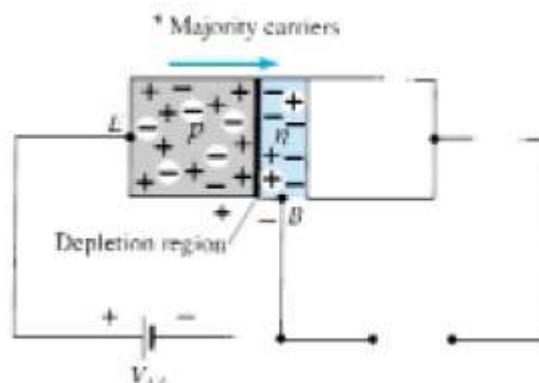

Figure 3.3 Forward-biased junction of a pnp transistor.