Common-Base Configuration (CB)
The CB configuration having a low input and high output impedance and a current gain less than 1, the voltage gain can be quite large, $r_o$ in MΩ so that ignored in parallel with $R_C$

\[ Z_i = R_E \parallel r_e \]  \[ Z_o = R_C \]  \[ A_v = \frac{V_o}{V_i} = \frac{\alpha R_C}{r_e} \approx \frac{R_i}{r_e} \]  \[ A_i = \frac{I_o}{I_i} = -\alpha \approx -1 \]

Phase Relationship: the resulting equation for the $A_v$ is a positive reveals that the output $V_o$ and input $V_i$ are in phase for the common-base configuration

Example 8: For the network in fig 6-24

\[ I_E = \frac{V_{EE} - V_{BB}}{R_E} = \frac{2 \text{ V} - 0.7 \text{ V}}{1 \text{ kΩ}} = \frac{1.3 \text{ V}}{1 \text{ kΩ}} = 1.3 \text{ mA} \]
\[ r_e = \frac{26 \text{ mV}}{I_F} = 26 \text{ mV} \times 1.3 \text{ mA} = 20 \Omega \]

\[ Z_i = R_e || r_e = 1 \text{ k}\Omega || 20 \Omega = 19.61 \Omega \equiv r_e \]

\[ Z_o = R_C = 5 \text{ k}\Omega \]

\[ A_v = \frac{R_C}{r_e} = \frac{5 \text{ k}\Omega}{20 \Omega} = 250 \]

\[ A_i = -0.98 = -1 \]

**Collector Feedback Configuration (CE)**

A feedback path from collector to base increased the stability of the system.

**Fig6-25 feedback configuration**

**Fig6-26 r_e model into network of fig6-25**

\[ l' = \frac{V_o - V_i}{R_F} \]

\[ V_o = -b I_b R_C = -b I_b R_C \]

\[ I_o = \beta I_b + l' \]

Since \( \beta I_b \) is normally much larger than \( l' \),

\[ I_o = \beta I_b \]

and

\[ V_o = -b \left( \frac{V_i}{\beta r_e} \right) R_C = -\frac{R_C}{r_e} V_i \]

\[ l' = \frac{V_o - V_i}{R_F} = \frac{V_o}{R_F} - \frac{V_i}{R_F} = -\frac{R_C V_i}{R_F} - \frac{V_i}{R_F} \left( 1 + \frac{R_C}{r_e} \right) \]

\[ V_i = I_b \beta r_e = (l_i + l') \beta r_e = I_b \beta r_e + l' \beta r_e \]

\[ V_i = \frac{1}{R_F} \left[ 1 + \frac{R_C}{r_e} \right] \beta r_e V_i \]

\[ V_i \left( 1 + \frac{\beta r_e}{R_F} \left[ 1 + \frac{R_C}{r_e} \right] \right) = I_b \beta r_e \]
and
\[ Z_o = \frac{V_i}{I_i} = \frac{\beta r_e}{1 + \frac{\beta r_e}{R_F} \left( 1 + \frac{R_C}{r_e} \right)} \]

but \( R_C \) is usually much greater than \( r_e \) and \( 1 + \frac{R_C}{r_e} \approx \frac{R_C}{r_e} \)
so that
\[ Z_o = \frac{\beta r_e}{1 + \frac{\beta R_C}{R_F}} \]

or
\[ Z_o = \frac{r_e}{1 + \frac{R_C}{\beta}} \]

\[ \text{[6-58]} \]

\( Z_o \) to define \( Z_o \) set \( V_i \) to zero, the effect of \( \beta r_e \) is removed and \( R_F \) appears in parallel with \( R_C \)

\[ \text{[6-59]} \]

\( A_v \) at node C of Fig 6-26
\[ I_o = \beta I_b + I' \]
values, \( \beta I_b \gg I' \) and \( I_o = \beta I_b \).
\[ V_o = -I_o R_C = -(\beta I_b) R_C \]
\[ I_b = \frac{V_o}{\beta r_e} \]
gives us
\[ V_o = -\beta \frac{V_i}{r_e} R_C \]
\[ A_v = \frac{V_o}{V_i} = -\frac{R_C}{r_e} \]

\[ \text{[6-60]} \]

\( A_i \) Applying KVL around the outside network loop
\[ V_i + V_{R_e} - V_o = 0 \]
\[ I_b \beta r_e + (I_b - I_i) R_F + I_i R_C = 0 \]
\[ I_o = \beta I_b \]
we have
\[ I_b \beta r_e + I_b R_F - I_R_F + \beta I_o R_C = 0 \]
\[ I_o (\beta r_e + R_F + \beta R_C) = I_R_F \]

\[ \text{noting} \ I_o = \frac{I_o}{\beta} \ \text{from} \ I_o = \beta I_b \ \text{yields} \]
\[ \frac{I_o}{\beta} (\beta r_e + R_F + \beta R_C) = I_R_F \]
\[ I_o = \frac{\beta R_C I_i}{\beta r_e + R_F + \beta R_C} \]
Ignoring $\beta r_e$ compared to $R_F$ and $\beta R_C$ gives us

\[
A_i = \frac{I_o}{I_i} = \frac{\beta R_F}{R_F + \beta R_C}
\]

[6-61]

$\beta R_C >> R_F$

\[
A_i = \frac{I_o}{I_i} = \frac{\beta R_F}{\beta R_C}
\]

\[
A_i = \frac{I_o}{I_i} = \frac{R_F}{R_C}
\]

[6-62]

**Phase Relationship**: the negative sign in the resulting equation for the $A_v$ reveals that a $180^\circ$ phase shift occurs between the output $V_O$ and input $V_i$

**Example 9**: For the network of fig 6-27 determine

\[
\begin{align*}
(a) & \quad r_e, \\
(b) & \quad Z_v, \\
(c) & \quad Z_{in}, \\
(d) & \quad A_{v}, \\
(e) & \quad A_{i},
\end{align*}
\]

**Solution:**

\[
I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta R_C} = \frac{9 \text{ V} - 0.7 \text{ V}}{180 \text{ k}\Omega + (200)(2.7 \text{ k}\Omega) = 11.53 \text{ mA}}
\]

\[
I_E = (\beta + 1)I_B = (201)(11.53 \text{ mA}) = 2.32 \text{ mA}
\]

\[
r_e = \frac{26 \text{ mV}}{2.32 \text{ mA}} = \frac{26 \text{ mV}}{2.32 \text{ mA}} = 11.21 \Omega
\]

\[
Z_i = \frac{r_e}{\beta R_F + R_C} = \frac{11.21 \Omega}{0.005 + 0.015} = 11.21 \Omega
\]

\[
Z_o = R_C || R_F = 2.7 \text{ k}\Omega || 180 \text{ k}\Omega = 2.66 \text{ k}\Omega
\]

\[
A_v = \frac{R_C}{r_e} = \frac{27 \text{ k}\Omega}{11.21 \Omega} = -240.86
\]

\[
A_i = \frac{\beta R_F}{R_F + \beta R_C} = \frac{200(180 \text{ k}\Omega)}{180 \text{ k}\Omega + (200)(2.7 \text{ k}\Omega)} = 50
\]
For the configuration of Fig6-28, will determine the variables

\[ Z_i = \frac{R_v}{1 + \frac{R_e}{R_f}} \]

\[ Z_o = R_C \parallel R_F \]

\[ A_v = \frac{R_C}{R_E} \]

\[ A_i = \frac{1}{\beta} \frac{1}{R_F} \left( R_F + \frac{1}{C_3} \right) \]

Collector DC feedback Configuration (CE)
The dc feedback resistor increased stability; \( C_3 \) will shift portions of the feedback resistance to the input and output sections of the network in the ac domain.

\[ Z_i = R_F \parallel \beta R_e \]

\[ Z_o = R_C \parallel R_F \parallel r_o \]

For \( r_o \geq 10R_C \)
For $r_o \geq 10R_C$

$$A_v = \frac{V_o}{V_i} \approx \frac{R_F || R_C}{r_o}$$

$A_v$ for the input side

$$I_o = \frac{R_F I_i}{R_F + \beta r_e} \quad \text{or} \quad \frac{I_o}{I_i} = \frac{R_F}{R_F + \beta r_e}$$

and for the output side using $R' = r_o || R_F$

$$I_o = \frac{R' \beta I_b}{R' + R_F} \quad \text{or} \quad \frac{I_o}{I_b} = \frac{R' \beta}{R' + R_F}$$

$$A_i = \frac{I_o}{I_i} \cdot \frac{I_b}{I_o} = \frac{R_F}{R_F + \beta r_e} \cdot \frac{r_o || R_F}{r_o || R_F + \beta r_e}$$

and

$$A_i = \frac{I_o}{I_i} = \beta \frac{R_F}{(R_F + \beta r_e)(R' + R_C)}$$

Since $R_F$ is usually much larger than $\beta r_e$, $R_F + \beta r_e \approx R_F$

and

$$A_i = \frac{I_o}{I_i} \approx \beta \frac{R_F}{R'_F(r_o || R_F + R_C)}$$

Or

$$A_i = \frac{I_o}{I_i} = -\frac{Z_i}{Z_o}$$

**Phase Relationship:** the negative sign in the resulting equation for the $A_v$ reveals that a 180° phase shift occurs between the output $V_o$ and input $V_i$. 

[6-69]

[6-70]

[6-71]

[6-72]

[6-73]

[6-74]
Example 10: For the network of fig6-31 determine:

(a) $r_e$
(b) $Z_o$
(c) $Z_i$
(d) $A_v$
(e) $A_p$

Solution: DC testing:

$I_B$

\[
I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta R_C} = \frac{12 \text{ V} - 0.7 \text{ V}}{(120 \text{ k}\Omega + 68 \text{ k}\Omega) + (140)3 \text{ k}\Omega} = \frac{11.3 \text{ V}}{608 \text{ k}\Omega} = 18.6 \mu\text{A}
\]

$I_E$

\[(\beta + 1)I_B = (141)(18.6 \mu\text{A}) = 2.62 \text{ mA}
\]

$r_e$

\[
r_e = \frac{26 \text{ mV}}{I_E} = \frac{26 \text{ mV}}{2.62 \text{ mA}} = 9.92 \Omega
\]

$\beta r_e$

\[(140)(9.92 \Omega) = 1.39 \text{ k}\Omega
\]

$Z_i$

\[Z_i = R_F || \beta r_e = 120 \text{ k}\Omega || 1.39 \text{ k}\Omega = 1.37 \text{ k}\Omega
\]

Testing the condition $r_o \geq 10R_C$ we find

\[30 \text{ k}\Omega \geq 10(3 \text{ k}\Omega) = 30 \text{ k}\Omega \quad \text{It is satisfied}
\]

So $Z_o$:

\[Z_o = R_C || R_{F_2} = 3 \text{ k}\Omega || 68 \text{ k}\Omega = 2.87 \text{ k}\Omega
\]

(d) $r_o \geq 10R_C$, therefore,

\[A_v \approx -\frac{R_{F_2} || R_C}{r_e} = -\frac{68 \text{ k}\Omega || 3 \text{ k}\Omega}{9.92 \Omega} = -\frac{2.87 \text{ k}\Omega}{9.92 \Omega} = -289.3
\]
Approximate Hybrid Equivalent Circuit

\[ h_{ie} = \beta r_e \]
\[ h_{fe} = \beta \]
\[ h_{oe} = 1/r_o \]
\[ h_{ib} = -\alpha \]
\[ h_{ib} = r_e \]

Fixed-Bias Configuration (CE)

\[ Z_i = R_B \parallel h_{ie} \]  \[ 6-75 \]
\[ Z_o = R_C \parallel 1/h_{oe} \]  \[ 6-76 \]
\[ A_v = \frac{V_o}{V_i} = \frac{h_{fe}(R_C \parallel 1/h_{oe})}{h_{ie}} \]  \[ 6-77 \]
\[ A_i = \frac{I_o}{I_i} = h_{ie} \]  \[ 6-78 \]

**Example 11:** For the network of fig6-37, determine
Solution:

(a) \( Z_i = R_0 \| h_{ie} = 330 \, \text{k}\Omega \| 1.175 \, \text{k}\Omega \)
    
    \[ Z_i = 1.171 \, \text{k}\Omega \]

(b) \( r_o = \frac{1}{h_{ro}} = \frac{1}{20 \, \mu\text{A/V}} = 50 \, \text{k}\Omega \)

\[ Z_o = \frac{1}{h_{ro}} || R_C = 50 \, \text{k}\Omega \| 2.7 \, \text{k}\Omega = 2.56 \, \text{k}\Omega = R_C \]

(c) \( A_v = \frac{h_{pa}(R_C \| 1/h_{ro})}{h_{ro}} = \frac{(120)(2.7 \, \text{k}\Omega || 50 \, \text{k}\Omega)}{1.171 \, \text{k}\Omega} = -262.34 \)

(d) \( A_i \equiv h_{re} = 120 \)

Voltage-Divider Configuration (CE bypassed)

\( R' = R_1 \| R_2 \)

\[ Z_i = R' \| h_{ie} \]

[6-79]

\[ Z_o \equiv R_C \]

[6-80]

\[ A_v = -\frac{h_{pa}(R_C \| 1/h_{ro})}{h_{ro}} \]

[6-81]

\[ A_i = \frac{h_{re}R'}{R' + h_{ir}} \]

[6-82]

Unbypassed Emitter-Bias Configuration (CE)

\( \beta r_e \) replaced by \( h_{ie} \) and \( \beta I_b \) by \( h_{re}I_b \). The analysis will proceed in the manner
**Fig 6-39 CE unbypassed emitter-bias configuration**

$Z_i$:  

\[ Z_i = h_{ie} R_E \]  

[6-83]

\[ Z_i = R_B \| Z_b \]  

[6-84]

$Z_o$  

\[ Z_o = R_C \]  

[6-89]

$A_v$  

\[ A_v = \frac{h_{ie} R_C}{Z_D} \approx \frac{h_{ie} R_C}{h_{fe} R_E} \]  

And  

\[ A_v = \frac{R_C}{R_E} \]  

[6-90]

$A_i$  

\[ A_i = -\frac{h_{ie} R_B}{R_B + Z_s} \]  

[6-91]

or  

\[ A_i = -A \frac{Z_i}{R_C} \]  

[6-92]

**Emitter-Follower Configuration (CE)**  

$\beta r_e = h_{ie}$ and $\beta = h_{fe}$, the resulting equations will therefore be quite similar.

$Z_i$:  

\[ Z_i = h_{ie} R_E \]  

[6-93]
The output network will appear as shown in fig 6-41:

\[ Z_i = R_E \parallel h_{ib} \]

or since \( 1 + h_{ib} = h_{je} \),

\[ Z_o = R_E \parallel \frac{h_{re}}{1 + h_{re}} \]

or since \( 1 + h_{ib} = h_{je} \),

\[ Z_v = \frac{R_E}{h_{je}} \]

\[ A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + h_{re}/(1 + h_{re})} \]

\[ A_i = \frac{h_{fe} R_B}{R_B + Z_b} \]

\[ A_i = -A_v \frac{Z_i}{R_E} \]

Common-Base Configuration (CB)

\[ Z_i = R_E \parallel h_{ib} \]

\[ Z_o = R_C \]

Fig 6-41 CB configuration

Fig 6-42 CB hybrid equivalent circuit
**Example 12:** For the network of fig6-43, determine:

**Solution:**

(a) \( Z_i = R_x || h_{ib} = 2.2 \text{ k}\Omega || 14.3 \text{ k}\Omega = 14.21 \text{ k}\Omega \approx h_{ib} \)

(b) \( r_n = \frac{1}{h_{ob}} = \frac{1}{0.5 \mu\text{A/V}} = 2 \text{ M}\Omega \)

\( Z_o = \frac{1}{h_{ob}} || R_C \equiv R_C = 3.3 \text{ k}\Omega \)

(c) \( A_v = \frac{h_{pb} R_C}{h_{ob}} = \frac{(-0.99)(3.3 \text{ k}\Omega)}{14.21} = 229.91 \)

(d) \( A_i \approx h_{ib} = -1 \)
Table 6-1 Relative Levels for the Important Parameters of the CE, CB, and CC Transistor Amplifier

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Z₁</th>
<th>Z₂</th>
<th>A₀</th>
<th>A₁</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixed-bias:</td>
<td>Medium (1 kΩ)</td>
<td>(Rₐ ≥ 10βrₑ)</td>
<td>Medium (2 kΩ)</td>
<td>(Rₐ ≥ 10Rₑ)</td>
</tr>
<tr>
<td></td>
<td>(Rₐ\beta_rₑ / \beta_rₑ / \beta_rₑ)</td>
<td>(Rₐ) / (rₑ)</td>
<td>High (−200)</td>
<td>((Rₑ / rₑ) / (rₑ / rₑ))</td>
</tr>
<tr>
<td></td>
<td>(Rₐ\beta_rₑ / \beta_rₑ / \beta_rₑ)</td>
<td>(Rₐ) / (rₑ)</td>
<td>High (100)</td>
<td>((Rₑ / rₑ) / (rₑ / rₑ))</td>
</tr>
<tr>
<td>Voltage-divider bias:</td>
<td>Medium (1 kΩ)</td>
<td>(Rₐ) / (rₑ)</td>
<td>Medium (2 kΩ)</td>
<td>(Rₐ) / (rₑ)</td>
</tr>
<tr>
<td></td>
<td>(Rₐ\beta_rₑ / \beta_rₑ / \beta_rₑ)</td>
<td>(Rₐ) / (rₑ)</td>
<td>High (−200)</td>
<td>((Rₑ / rₑ) / (rₑ / rₑ))</td>
</tr>
<tr>
<td></td>
<td>(Rₐ\beta_rₑ / \beta_rₑ / \beta_rₑ)</td>
<td>(Rₐ) / (rₑ)</td>
<td>High (50)</td>
<td>((Rₑ / rₑ) / (rₑ / rₑ))</td>
</tr>
<tr>
<td>Unbypassed emitter bias:</td>
<td>High (100 kΩ)</td>
<td>(Rₑ / rₑ)</td>
<td>Medium (2 kΩ)</td>
<td>(Rₑ / rₑ)</td>
</tr>
<tr>
<td></td>
<td>(Rₐ\beta_rₑ / \beta_rₑ / \beta_rₑ)</td>
<td>(Rₐ) / (rₑ)</td>
<td>Low (−5)</td>
<td>((Rₑ / rₑ) / (Rₑ / rₑ))</td>
</tr>
<tr>
<td></td>
<td>(Rₐ\beta_rₑ / \beta_rₑ / \beta_rₑ)</td>
<td>(Rₐ) / (rₑ)</td>
<td>High (50)</td>
<td>((Rₑ / rₑ) / (Rₑ / rₑ))</td>
</tr>
<tr>
<td>Emitter-follower:</td>
<td>High (100 Ω)</td>
<td>(Rₑ / rₑ)</td>
<td>Low (20 Ω)</td>
<td>(Rₑ / rₑ)</td>
</tr>
<tr>
<td></td>
<td>(Rₐ\beta_rₑ / \beta_rₑ / \beta_rₑ)</td>
<td>(Rₐ) / (rₑ)</td>
<td>Low (1)</td>
<td>((Rₑ / rₑ) / (Rₑ / rₑ))</td>
</tr>
<tr>
<td></td>
<td>(Rₐ\beta_rₑ / \beta_rₑ / \beta_rₑ)</td>
<td>(Rₐ) / (rₑ)</td>
<td>High (50)</td>
<td>((Rₑ / rₑ) / (Rₑ / rₑ))</td>
</tr>
<tr>
<td>Common-base:</td>
<td>Low (20 Ω)</td>
<td>(Rₑ / rₑ)</td>
<td>Medium (2 kΩ)</td>
<td>(Rₑ / rₑ)</td>
</tr>
<tr>
<td></td>
<td>(Rₐ\beta_rₑ / \beta_rₑ / \beta_rₑ)</td>
<td>(Rₐ) / (rₑ)</td>
<td>High (200)</td>
<td>((Rₑ / rₑ) / (Rₑ / rₑ))</td>
</tr>
<tr>
<td></td>
<td>(Rₐ\beta_rₑ / \beta_rₑ / \beta_rₑ)</td>
<td>(Rₐ) / (rₑ)</td>
<td>Low (−1)</td>
<td>((Rₑ / rₑ) / (Rₑ / rₑ))</td>
</tr>
<tr>
<td>Collector feedback:</td>
<td>Medium (1 kΩ)</td>
<td>(rₑ) / (Rₑ)</td>
<td>Medium (2 kΩ)</td>
<td>(rₑ) / (Rₑ)</td>
</tr>
<tr>
<td></td>
<td>(rₑ / (Rₑ / Rₑ))</td>
<td>(rₑ) / (Rₑ)</td>
<td>High (−200)</td>
<td>((rₑ) / (Rₑ / Rₑ))</td>
</tr>
<tr>
<td></td>
<td>(rₑ / (Rₑ / Rₑ))</td>
<td>(rₑ) / (Rₑ)</td>
<td>High (50)</td>
<td>((rₑ) / (Rₑ / Rₑ))</td>
</tr>
</tbody>
</table>
SUMMARY

Important Conclusions and Concepts

1. The $r_e$ model for a BJT in the ac domain is sensitive to the actual dc operating conditions of the network. This parameter is normally not provided on a specification sheet, although $h_{ie}$ of the normally provided hybrid parameters is equal to $\beta r_e$ but only under specific operating conditions.

2. Most specification sheets for BJT include a list of hybrid parameters to establish an ac model for the transistor. One must be aware, however, that they are provided for a particular set of dc operating conditions.

3. The CE fixed-bias configuration can have a significant voltage gain characteristic, although its input impedance can be relatively low. The approximate current gain is given by simply beta, and the output impedance is normally assumed to be $R_c$.

4. The voltage-divider bias configuration has a higher stability than the fixed-bias configuration, but it has about the same voltage gain, current gain, and output impedance. Due to the biasing resistors, its input impedance may be lower than that of the fixed-bias configuration.

5. The CE emitter-bias configuration with an unbypassed emitter resistor has a larger input resistance than the bypassed configuration, but it will have a much smaller voltage gain than the bypassed configuration. For the unbypassed or by-passed situation, the output impedance is normally assumed to be simply $R_c$.

6. The emitter-follower configuration will always have an output voltage slightly less than the input signal. However, the input impedance can be very large, making it very useful for situations where a high-input first stage is needed to "pick up "as much of the applied signal as possible. Its output impedance is extremely low, making it an excellent signal source for the second stage of a multistage amplifier.

7. The common-base configuration has very low input impedance, but it can have a significant voltage gain. The current gain is just less than 1, and the output impedance is simply $R_c$.

8. The collector feedback configuration has input impedance that is sensitive to beta and that can be quite low depending on the parameters of the configuration. However, the voltage gain can be significant and the current gain of some magnitude if the parameters are chosen properly. The output impedance is most often simply the collector resistance $R_c$.

9. The collector dc feedback configuration utilizes the dc feedback to increase its stability and the changing state of a capacitor from dc to ac to establish a higher voltage gain than obtained with a straight feedback connection. The output impedance is usually close to $R_c$ and the input impedance relatively close to that obtained with the basic common-emitter configuration.

10. The approximate hybrid equivalent network is very similar in composition to that used with the $r_e$ model. In fact, the same methods of analysis can be applied to both models. For the hybrid model the results will be in terms of the network parameters and the hybrid parameters, whereas for the $r_e$ model they will be in terms of the network parameters and $\beta$ , $r_e$ and $r_o$.

11. The hybrid model for common-emitter, common-base, and common-collector configurations is the same. The only difference will be the magnitude of the parameters of the equivalent network.
12. for BJT amplifiers that fail to operate properly, the first step should be checking the dc level and be sure that they support the dc operation of the design.

13. Always keep in mind that capacitors are typically open circuits for the dc analysis and operation and essentially short circuits for the ac response

**Equations**

**CE fixed bias:**

\[
Z_i = \beta r_e \\
Z_o = R_C \\
A_v = \frac{R_C}{r_e} \\
A_i = -A_v \frac{Z_i}{R_C} = \beta
\]

**CE Voltage-divider bias:**

\[
Z_i = \frac{R_1 R_2}{R_1 + R_2 + \beta r_e} \\
Z_o = R_C \\
A_v = \frac{R_C}{r_e} \\
A_i = -A_v \frac{Z_i}{R_C} = \beta
\]

**CE emitter-bias:**

\[
Z_i \approx R_B || \beta R_E \\
Z_o \approx R_C \\
A_v \approx \frac{R_C}{R_E} \\
A_i \approx \frac{\beta R_B}{R_B + \beta R_E}
\]

**Emitter-follower:**

\[
Z_i \approx R_B || \beta R_E \\
Z_o \approx r_e \\
A_v \approx 1 \\
A_i = -A_v \frac{Z_i}{R_E}
\]

**Common-base:**

\[
Z_i \approx R_E || r_e \\
Z_o \approx R_C \\
A_v \approx \frac{R_C}{r_e} \\
A_i \approx -1
\]
Collector feedback:

\[ Z_i \approx \frac{r_e}{1 + \frac{R_C}{\beta R_F}} \]

\[ Z_o \approx R_C \| R_F \]

\[ A_v = \frac{R_C}{r_e} \]

\[ A_i \approx \frac{R_F}{R_C} \]

Collector dc feedback:

\[ Z_i \approx R_{F_1} \| \beta r_e \]

\[ Z_o \approx R_C \| R_{F_2} \]

\[ A_v = -\frac{R_{F_2} \| R_C}{r_e} \]

\[ A_i = -A_v \frac{Z_i}{R_C} \]
7-Felid Effect Transistor (FET)

BJT is a current-controlled device; that is $I_B$ controls $I_C$. The FET is a voltage-controlled device in which the voltage gate $V_G$ controls current through the device. FET is a three-terminal device containing one p-n junction built as either a Junction FET (JFET) or a Metal-Oxide Semiconductor FET (MOS-FET).

Construction and Characteristics of JFETS

JFET is a type of FET that operates with a reverse biased junction to control current in the channel. JFETs either n channel or p channel.

![Fig7-1 basic structure of the two types of JFET](image1)

![Fig7-2 Water analogy for the JFET control mechanism](image2)

**JFET Symbols**

Notice that the arrow on the gate points "in" for n-channel and "out" for p channel.

![Fig7-3 JFET symbols (a) n-channel (b) p-channel](image3)

**JFET Characteristics**

First consider the case where the $V_{GS} = 0V$ Fig7-4a as $V_{DD}$ (and thus $V_{DS}$) is increased from 0V, $I_D$ will increase proportionally (Fig7-4b between points A and B), this region is called the ohmic region because $V_{DS}$ and $I_D$ are related by Ohm’s law.

Point B in Fig7-4b $I_D$ becomes constant. As $V_{DS}$ increases from point B to point C, the reverse-bias voltage in $V_{GD}$ produces a depletion region large enough to offset the increase in $V_{DS}$, thus keeping $I_D$ relatively constant.

**Pinch-Off Voltage $V_P$:** is the value of $V_{DS}$ at which $I_D$ becomes constant and $V_{GS} = 0V$, a continued increase in $V_{DS}$ above the $V_P$ voltage produces a constant drain current $I_{DSS}$ (Drain to Source current with gate sorted).

$I_{DSS}$ is the maximum drain current and is always specified on JFET data sheets, is defined by the condition $V_{GS} = 0V$ and $V_{DS} > |V_P|$

**Breakdown:** occurs at point C when $I_D$ begins to increase very rapidly with any further increase in $V_{DS}$, Breakdown result damage to the device, so JFETs are always operated below breakdown (between B & C).

$V_{GS}$ **Controls $I_D$:** Connect a bias voltage $V_{GG}$, as $V_{GS}$ is set to increasingly more negative values by adjusting $V_{GG}$, $I_D$ decreases.
Fig 7-4 the drain characteristic curve of a JFET for $V_{GS} = 0$ V, (pinch-off)

Fig 7-5 pinch-off occurs at a lower $V_{DS}$ as $V_{GS}$ is increased to more negative values

Cutoff Voltage $V_{GS(off)}$: the value of $V_{GS}$ that makes $I_D$ approximately zero, JFET must be operated between $V_{GS} = 0$ V and $V_{GS(off)}$, for this range of voltage $I_D$ will vary from a maximum ($I_{DSS}$) to a minimum. $V_{GS(off)}$ & $V_P$ are always equal in magnitude but **opposite in sign**

(a) $V_{GS} = 0$ V, $I_D = I_{DSS}$

(b) cutoff ($I_D = 0$A) $V_{GS}$ less than (more negative) $V_P$

(c) $I_D$ exists between 0A and $I_{DSS}$ for $V_{GS}$ less than or equal to 0V and greater than the $V_P$
The basic operation of a p-channel JFET is the same as for an n-channel device expect that is requires a negative $V_{DD}$ and a positive $V_{GS}$.

**Example 1:** JFET in fig $V_{GS(0ff)} = -3.5V$ & $I_{DSS} = 6mA$. Determine the minimum value of $V_{DD}$ required putting the device in the constant-current region of operation

**Solution:**

Since $V_{GS(0ff)} = -3.5V$, $V_F = 3.5$, $V_{DS} = 3.5V$, $I_D = I_{DSS} = 6mA$

$V_{RD} = (6mA)(560\Omega) = 3.36V$

Applying KVL, $V_{DD} = V_{DS} + V_{RD} = 3.5V + 3.36V = 6.86V$

**JFET Input Resistance**
The input resistance at the gate is very high. JFET data sheets often specify the input resistance by giving a value for the gate reverse current $I_{GSS}$ at a certain $V_{GS}$

**Example 2:** A certain JFET has an $I_{GSS}$ of 1nA for $V_{GS} = -20V$. Determine the input resistance

**Solution:**

Voltage-Controlled Resistor
In ohmic region JFET be employed as a variable resistor whose resistance is controlled by $V_{GS}$

$r_o = \frac{r_d}{1 - \frac{V_{GS}}{V_P}}$  \[7-1\]

$r_o$ is the resistance with $V_{GS} = 0V$, and $r_d$ the resistance at a particular level of $V_{GS}$

**Transistor Characteristic**
**Derivation:** For BJT the output current $I_C$ and input controlling current $I_B$ related to beta, which was considered constant for the analysis

$A liner relationship exist between I_C and I_B$.  \[7-2\]
This liner relationship does not exist between the output and input quantities of the JFET, the relationship between $I_D$ and $V_{GS}$ is defined by **Shockley’s equation**:

\[ I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 \]

The transfer characteristics defined by Shockley’s equation are unaffected by the network in which the device is employed.

When $V_{GS} = 0V$, $I_D = I_{DSS}$

When $V_{GS} = V_T = -4V$, $I_D = 0 mA$, defining an other point on transfer curve. Applying Shockley’s Equation: Eq[7-3] Substituting $V_{GS} = 0V$ gives

\[ I_D = I_{DSS} \left( 1 - \frac{0}{V_P} \right)^2 = I_{DSS}(1 - 0)^2 \]

Substituting $V_{GS} = -1V$ yields

\[ I_D = I_{DSS} \left( 1 - \frac{-1}{V_P} \right)^2 = I_{DSS}(1 - \frac{1}{4})^2 = I_{DSS}(0.75)^2 \]

\[ I_D = 4.5 mA \]

The derivation is quite straightforward and will result in

\[ V_{GS} = V_T \left( 1 - \frac{I_D}{I_{DSS}} \right) \]

Test Eq[7-6] by finding $V_{GS}$ that will result in a drain current of 4.5mA in fig7-8

\[ V_{GS} = -4 V \left( 1 - \sqrt{\frac{4.5 mA}{8 mA}} \right) = -4 V(1 - \sqrt{0.5625}) = -4 V(1 - 0.75) = -4 V(0.25) = -1 V \]
Shorthand Method

We can have a shorthand method as following: if we specify \( V_{GS} \) to be \( 1/2 \) \( V_P \) the resulting level of \( I_D \) will be the following, as determine by Shockley’s equation

\[
I_D = I_{DSS} \left( 1 - \frac{V_{GS}^2}{V_P^2} \right) = I_{DSS} \left( 1 - \left( \frac{1}{2} \right)^2 \right) = I_{DSS} \left( 1 - 0.25 \right) \]

And

\[
I_D \quad \text{for} \quad V_{GS} = \frac{V_P}{2} = -4V/2 = -2V, \quad \text{if we choose} \quad I_D = \frac{I_{DSS}}{2} \quad \text{& substitute into Eq}[7-6] \]

\[
V_{GS} = V_P \left( 1 - \sqrt{1 - \frac{I_D}{I_{DSS}}} \right) = V_P \left( 1 - \sqrt{\frac{I_{DSS}/2}{I_{DSS}}} \right) = V_P \left( 1 - \sqrt{0.5} \right) = V_P \left( 0.293 \right) \]

Example 3: Sketch the transfer curve defined by \( I_{DSS} = 12mA \) and \( V_P = -6V \)

Solution:

Two plot points are defined by

\[
I_{DSS} = 12 \text{ mA} \quad \text{and} \quad V_{GS} = 0 \text{ V} \]

and

\[
I_D = 0 \text{ mA} \quad \text{and} \quad V_{GS} = V_P \]

At \( V_{GS}=V_P/2 = -6V/2 = -3V \) then \( I_{DSS}/4 = 12mA/4 = 3mA \).

At \( I_D=I_{DSS}/2=12mA/2=6mA \) the \( V_{GS} = 0.3V_P = 0.3(-6V) = -1.8V \)

For p-channel \( V_P \) & \( V_{GS} \) will be positive and the curve will be the mirror image of the transfer curve obtained with an n-channel and the same limiting values

Example 4: Sketch the transfer curve for a p-channel device with \( I_{DSS} = 4mA \) and \( V_P = 3V \)

Solution: At \( V_{GS} = V_P/2 = 3V/2 = 1.5V, I_D=I_{DSS}/4 = 4mA/4 = 1mA \)

At \( I_D= I_{DSS}/2=4mA/2=2mA, V_{GS} = 0.3V_P = 0.3(3V) = 0.9V \)

transfer curve for the p-channel device of Ex 4:
Important Relationships

MOSFET (metal-oxide-semiconductor-field-effect transistor)
There is no direct electrical connection between the gate terminal and the channel of a MOSFET; it is the insulating layer of SiO\textsubscript{2} in the MOSFET construction that accounts for the very desirable high input impedance of the device,

Depletion MOSFET (D-MOSFET)
The drain and source are diffused into the substrate material then connected by a narrow channel adjacent to the insulated gate.

Depletion Mode
Visualize the gate as one plate of a parallel plate capacitor and the channel as the other plate. The SiO\textsubscript{2} insulating layer is the dielectric. With V\textsubscript{GS} negative voltage, the negative charges on the gate repel conduction electrons from the channel, leaving positive ions in their place. Thus decreasing the channel conductivity. The greater the negative voltage (V\textsubscript{GS}), the greater the depletion of n-channel electrons, at a V\textsubscript{GS(off)} the channel is totally depleted and I\textsubscript{D} is zero. In depletion mode current between drain and source will result from a voltage connected across the drain-source.
Like the n-channel JFET, the n-channel D-MOSFET conducts $I_D$ for $V_{GS}$ between $V_{GS(off)}$ and 0V. The D-MOSFET conducts for values of $V_{GS}$ above 0 V.

**D-MOSFET Symbols**

**P-channel Depletion-Type MOSFET**

**Example 3:** Sketch the transfer characteristics for n-D-MOSFET with $I_{DSS} = 10mA$ and $V_P = -4V$

**Solution:**

At $V_{GS} = 0 \text{ V}$, $I_D = I_{DSS} = 10 \text{ mA}$

$V_{GS} = V_P = -4 \text{ V}$, $I_D = 0 \text{ mA}$

$V_{GS} = \frac{V_P}{2} = -2 \text{ V}$, $I_D = \frac{I_{DSS}}{4} = \frac{10 \text{ mA}}{4} = 2.5 \text{ mA}$

and at $I_D = \frac{I_{DSS}}{2}$, $V_{GS} = 0.3V_P = 0.3(-4 \text{ V}) = -1.2 \text{ V}$
$I_D$ increases very rapidly with increasing positive values of $V_{GS}$. So that choice values to be substituted into Shockley's equation. In this case, we will try +1V as follows:

![Diagrams of MOSFETs](image)

**Enhancement Mode**

With a positive $V_{GS}$, more conduction electrons are attracted into the channel, thus increasing (enhancing) the channel conductivity,

**Enhancement MOSFET (E-MOSFET)**

This type operates only in the enhancement mode and has no depletion mode. It has no structural channel.

For $n$-channel device, a positive $V_{GS}$ voltage above $V_{GS(off)}$ (threshold voltage) creating a thin layer of negative charges in the substrate region adjacent to the SiO$_2$ layer, the conductivity of the channel is enhanced by increasing the $V_{GS}$ voltage, thus pulling more electrons into the channel. For any $V_{GS}$ voltage below the threshold value, there is no channel.

\[
V_{DE} = V_{DS} - V_{GS}
\]

\[
V_{DS} = V_{GS} - V_T
\]

For values of $V_{GS}$ less than the threshold level, $I_D = 0mA$

\[
I_D = k(V_{GS} - V_T)^3
\]
Substituting $I_{P(n)} = 10 \text{ mA}$ when $V_{GS(n)} = 8 \text{ V}$ from the characteristics

$$k = \frac{10 \text{ mA}}{(8 \text{ V} - 2 \text{ V})^2} = \frac{10 \text{ mA}}{36 \text{ V}^2} = 0.278 \times 10^{-3} \text{ A/V}^2$$

and a general equation for $I_D$ for the characteristics of Fig. 7-16:

$$I_D = 0.278 \times 10^{-3}(V_{GS} - 2 \text{ V})^2$$

Substituting $V_{GS} = 4 \text{ V}$, we find that

$$I_D = 0.278 \times 10^{-3}(4 \text{ V} - 2 \text{ V})^2 = 0.278 \times 10^{-3}(2)^2$$

$$= 0.278 \times 10^{-3}(4) = 1.11 \text{ mA}$$

First, a horizontal line is drawn at $I_D = 0 \text{ mA}$ from $V_{GS} = 0 \text{ V}$ to $V_{GS} = 4 \text{ V}$ as in fig 7-18a next, a level of $V_{GS}$ greater than $V_T$ such as 5V is chosen and substituted into Eq.[7-13] to determine the resulting level of $I_D$ as follows:

$$I_D = 0.5 \times 10^{-3}(V_{GS} - 4 \text{ V})^2$$

And a point on the plot is obtained as in fig7-18b, finally, additional levels of $V_{GS}$ are chosen and the resulting levels of $I_D$ obtained. In particular, at $V_{GS} = 6, 7, \text{ and } 8 \text{ V}$, the level of $I_D$ is 2, 4.5, and $8 \text{ mA}$, respectively, as shown on the resulting plot of fig7-18
Example 4: $V_{GS(TH)} = 3\text{V}$, determine the resulting value of $k$ for MOSFET, the transfer characteristics.

**Solution:**

$$k = \frac{I_{D(on)}}{(V_{GS(TH)} - V_{DS(TO)})^2}$$

$$= \frac{3\text{mA}}{(10\text{V} - 3\text{V})^2} - \frac{3\text{mA}}{(7\text{V})^2} = \frac{3 \times 10^{-3}}{49} \text{A/V}^2$$

$$I_D = k(V_{GS} - V_T)^2$$

For $V_{GS} = 5\text{V}$,

$$I_D = 0.061 \times 10^{-3}(5\text{V} - 3\text{V})^2 = 0.061 \times 10^{-3}(2\text{V})^2$$

$$= 0.061 \times 10^{-3}(4) = 0.244\text{mA}$$

For $V_{GS} = 8, 10, 12, 14\text{V}$, $I_D$ will be 1.525, 3, 4.94, 7.38mA respectively.

Solution to Example 4:
CMOS

CMOS is a complementary MOSFET constructed by a p-channel and an n-channel MOSFET on the same substrate. P-channel on the left and the n-channel on the right.

One very effective use of the CMOS is as an inverter as shown in Fig7-21.

**SUMMARY TABLE**

<table>
<thead>
<tr>
<th>Type</th>
<th>Symbolic Representation</th>
<th>Transfer Curve</th>
<th>Input Resistance and Capacitance</th>
</tr>
</thead>
</table>
| JFET (n-channel)       | ![JFET Symbol]          | ![Transfer Curve] | R_i > 100 MΩ  
C_g: (1 – 10) pF |
| Depletion MOSFET (n-channel) | ![MOSFET Symbol] | ![Transfer Curve] | R_i > 10^3 Ω  
C_g: (1 – 10) pF |
SUMMARY

1. A current controlled device is one in which a current defines the operating condition of the device, whereas a voltage-controlled device is one in which a particular voltage defines the operating conditions.

2. Transistors are used as either amplifying devices or switching devices.

3. A field-effect transistor (FET) has three terminals: source, drain, and gate.

4. A junction field-effect transistor (JFET) operates with a reverse-biased gate-to-source pn junction. JFETs have very high input resistance due to the reverse-biased gate-source junction.

5. JFET current between the drain and the source is through a channel whose width is controlled by the amount of reverse bias on the gate-source junction.

6. The two types of JFETs are n-channel and p-channel.

7. The JFET can actually be used as a voltage-controlled resistor because of a unique sensitivity of the drain-to-source impedance to the gate-to-source voltage.

8. The maximum current for any JFET is labeled $I_{DSS}$ and occurs when $V_{GS} = 0V$.

9. The maximum current for a JFET occurs at pinch-off defined by $V_{GS} = V_P$.

10. The relationship between the drain current and the gate-to-source voltage of a JFET is nonlinear one defined by Shockley’s equation. As the current level approaches $I_{DSS}$, the sensitivity of $I_D$ to changes in $V_{GS}$ increases significantly.

11. The transfer characteristics ($I_D$ versus $V_{GS}$) are characteristics of the device itself and not sensitive to the network in which the JFET is employed.

12. When $V_{GS} = V_P/2$, $I_D = I_{DSS}/4$; and at a point where $I_D = I_{DSS}/2$, $V_{GS} = 0.3$ V.

13. Maximum operating conditions are determined by the product of the drain-to-source voltage and the drain current.

14. Metal-oxide semiconductor field-effect transistors (MOSFETs) differ from JFETs in that the gate of a MOSFET is insulated from the channel.

15. MOSFET is available in one of two types: depletion and enhancement.
16. The depletion-type MOSFET has the same transfer characteristics as a JFET for drain current up to the $I_{DSS}$ level. At this point the characteristics of a depletion-type MOSFET continue to levels above $I_{DSS}$, whereas those of the JFET will end.

17. A depletion/enhancement MOSFET (D-MOSFET) can operate with a positive, negative, or zero gate-to-source voltage.

18. The D-MOSFET has a physical channel between the drain and the source.

19. The arrow in the symbol of n-channel JFET or MOSFET will always point in to the center of the symbol, whereas those of a p-channel device will always point out of the center of the symbol.

20. An enhancement-only MOSFET (E-MOSFET) can operate only when the gate-to-source voltage exceeds a threshold value.

21. The E-MOSFET has no physical channel.

22. The transfer characteristics of an enhancement-type MOSFET are not defined by Shockley's equation but rather by a nonlinear equation controlled by the gate-to-source voltage, the threshold voltage, and a constant $k$ defined by the device employed. The resulting plot of $I_D$ versus $V_{GS}$ is one that rises exponentially with increasing values of $V_{GS}$.

23. A CMOS (complementary MOSFET) device is one that employs a unique combination of a p-channel and an n-channel MOSFET with a single set of external leads. It has the advantages of very high input impedance, fast switching speeds, and low operating power levels, all of which make it very useful in logic circuits.

**EQUATIONS: FET**

For a MOSFET (enhancement):

$$I_D = k(V_{GS} - V_T)^2$$

$$k = \frac{I_{D(rem)}}{(V_{GS(rem)} - V_T)^2}$$