Abstract

Reed Solomon codes are Powerful non binary error correcting codes. This code has wide use in wireless Communications and digital recoding. This research focused on burst errors that most occur in wireless communications .RS codes used in digital communication system have code symbols from Galois fiel (2^m) . Each symbol is made up of m bits. A (t) error correcting RS code has the following parameters : block length :n=2m-1, number of parity symbols :n-k=2t, k represents the number of data symbols, t refers to number of symbols that can be corrected . In this thesis, first the prototyping of a (255,239) RS codec (encoder and decoder) operates over GF (2^8) was described .

Hence every codeword comprises 239 information symbols, 16 symbols of which for parity and each symbol is represented by (8bit).This code can therefore correct up to 8 symbol errors in each codeword. The RS code was initially implemented using a computer . However in order to reduce the size and power requirement of the system and to increase the data rate we choose FPGA because of its ability to reconfigurable , relative low cost and fast designing computer.

The architecture of RS codec is consisted of encoding and decoding section generating RS code and decoding section generating corrected of the decoders are more complicated. The decoding algorithm comprised four distinct sub – process: syndrome calculation, calculation of the error locator polynomial, generation of the error pattern, and calculation of these error patterns through inverse transform. These error patterns were than added to the received word to obtain the estimated original information word.

FPGA's and other reprogrammable devices are suitable for algorithm realization. Hence in this thesis The RS codec was designed using model SIM (SE4.1i) VHDL.This induced the design that based on gate circuits for simulation, and implemented on Xilinx FPGA.The results of such design that presented here demonstrate how FPGAs can be used to provide the flexibility and performance and better resource utilization which meeting the speed and area constraints set by particular design.

Recapitulation of each process in the encoder and decoder are :encoder : frequruncy of operation =1/2.774ns, number of Slice Flip Flops:128 out of 3,072 , number of 4 input LUTs: 205 out of 3,072 , , number of occupied Slices:104out of 1,536, number of bonded IOBs: 19 out of 92 , total equivalent gate count for design: 2,257, and peak Memory Usage: 70 MB,

Decoder: frequruncy of operation = 1/6.385ns, number of Slice Flip Flops: 136 out of 1, 536, total number 4 input LUTs: 378 out of 1,536,
number used as LUTs: 371 ,number used as a route-thru: 7 ,number of External IOBs: 53 out of 180, number of SLICEs 205 out of 768, total equivalent gate count for design: 3,521

This research describes how to design RS codec on FPGA and many difficulties we have met in using FPGA.