University of Technology
Laser & Optoelectronics Engineering Department
Final Examination 2011/2012

Subject: Microprocessors *Class: 4th year*
Branch: Laser & Optoelectronic *Time: 3 hours*
Examiner: Dr. Sinan Majid AL-Yass *Date: 3 / 6 / 2012*

Attempt five questions only

Q_{1A}) **Using one Full Adder and one NAND gate; design combinational circuit with three inputs x, y, and z, and three outputs A, B, and C. When the binary input is 0, 1, 2, or 3 the binary output is one greater than the input. When the binary input is 4, 5, 6 or 7 the binary output is one less than the input?** *(10MARKS)*

Q_{1B}) **Write a microprocessor program (in assembly language) and draw a flow chart which simulate the operation of a half wave rectifier with gain equal to 2 for array of data stored in memory starting at address 3000_H and ending at $30FF_H$. Use shift method to test the sign of numbers?** *(10MARKS)*

Q_{2A}) **Illustrate the step-by-step conversion from analog to digital using four bits successive approximation ADC of a constant input voltage equal to 5.1 volt and a full scale DAC output equal to 16 volt?** *(10MARKS)*

Q_{2B}) **Consider a data written state, List the six steps that the microprocessor need to communicate with a memory?** *(10MARKS)*

Q_{3A}) **Simplify the following Boolean function using Karnaugh map:**

$$F = \overline{A}BC\overline{E} + \overline{A}BC\overline{D} + \overline{B}D\overline{E} + \overline{B}C\overline{D} + CD\overline{E} + BD\overline{E} + DE + \overline{B}C$$ *(10MARKS)*

Q_{3B}) **Explain cycle stealing DMA?** *(10 MARKS)*

Q_{4A}) **Use (4×1) multiplexer to implement the following function by taking (A and E) as select lines $F = \sum 1, 20, 3, 19, 4, 17, 6, 16, 7.$** *(10MARKS)*

Q_{4B}) **Explain pending interrupts, list interrupts according to their priorities?** *(10MARKS)*

Q_{5A}) **Design a counter with the irregular repeated binary count sequence as: $F=\sum 0, 1, 3, 7, 6, 4$ Use T- flip flops.** *(10MARKS)*

Q_{5B}) **Write a microprocessor program and draw a flow chart for a program which allows you to find the maximum number of array stored at location starting at $A0F9_H$ the array consist of 100 elements?** *(10MARKS)*

Q_{6A}) **Design a code converter that converts a decimal digit from the 8 4 -2 -1 code to BCD?**

Hint: The 8 4 -2 -1 code: [0000, 0111, 0110, 0101, 0100, 1011, 1010, 1001, 1000, 1111]
(10MARKS)

Q_{6B}) **List and plot the all signals group for the 8085 microprocessor?** *(10MARKS)*

Good luck

الأربعاء عام ٢٠١٢ ديسمبر ١٥

Wednesday **15 December**

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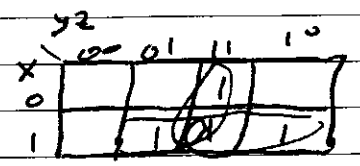
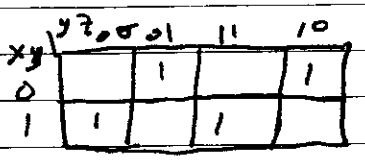
Q_{1A} :-

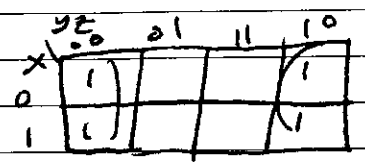
Dec	x	y	z	o/p	a	b	c
0	0	0	0	1	0	0	1
1	0	0	1	2	0	1	0
2	0	1	0	3	0	1	1
3	0	1	1	4	1	0	0
4	1	0	0	3	0	1	1
5	1	0	1	4	1	0	0
6	1	1	0	5	1	0	1
7	1	1	1	6	1	1	0



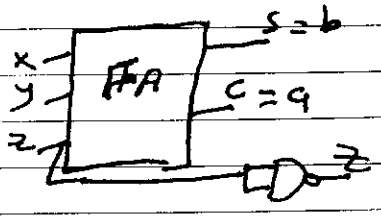
$a = yz + xz + xy$



$b = x \oplus y \oplus z$



$c = \bar{z}$



```
Q1EB
    LXI H,3000H
    LXI B,0100H
*** MOV A,M
    RAL
    JNC *
    MVI A,00H
    JMP **
*   RAR
    RLC          x2 gain
**  MOV M,A
    INX H
    DCX B
    JNZ ***
    RST1
```

00 for 5.1 volt ⇒ o/p = 0101

Q2A

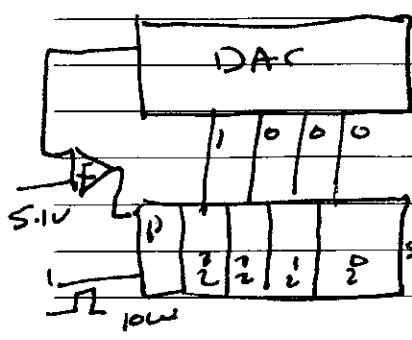
For 2^3 (MSB) ⇒ v_o = 8 volt

2^2 bit ⇒ v_o = 4 volt

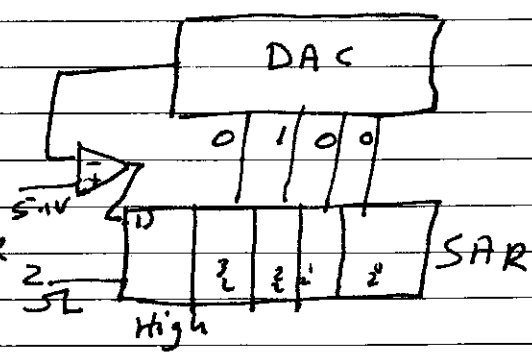
2^1 bit ⇒ v_o = 2 volt

2^0 bit ⇒ v_o = 1 volt (LSB)

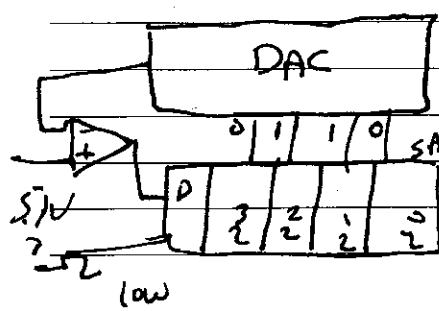
a) MSB trial



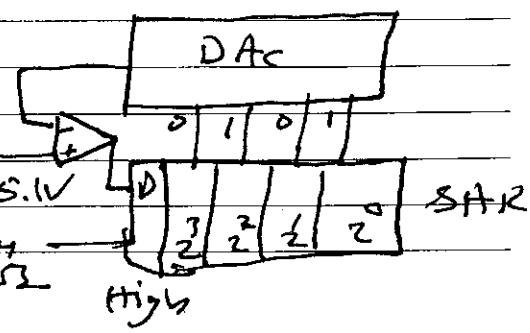
b) keep



c) Reset



d) keep



Q23

To communication with a memory, for example to read instruction from memory location:-

1- Mp placed 16-bit address on address bus.

2- The address on the bus is decoded by an external logic circuit.

3- The memory location is identified.

4- The Mp sends a pulse called memory read as control signal.

5- The pulse activates the memory chip.

6- The contents of the memory location (8-bit data) are placed on the data bus as in fig. (2).

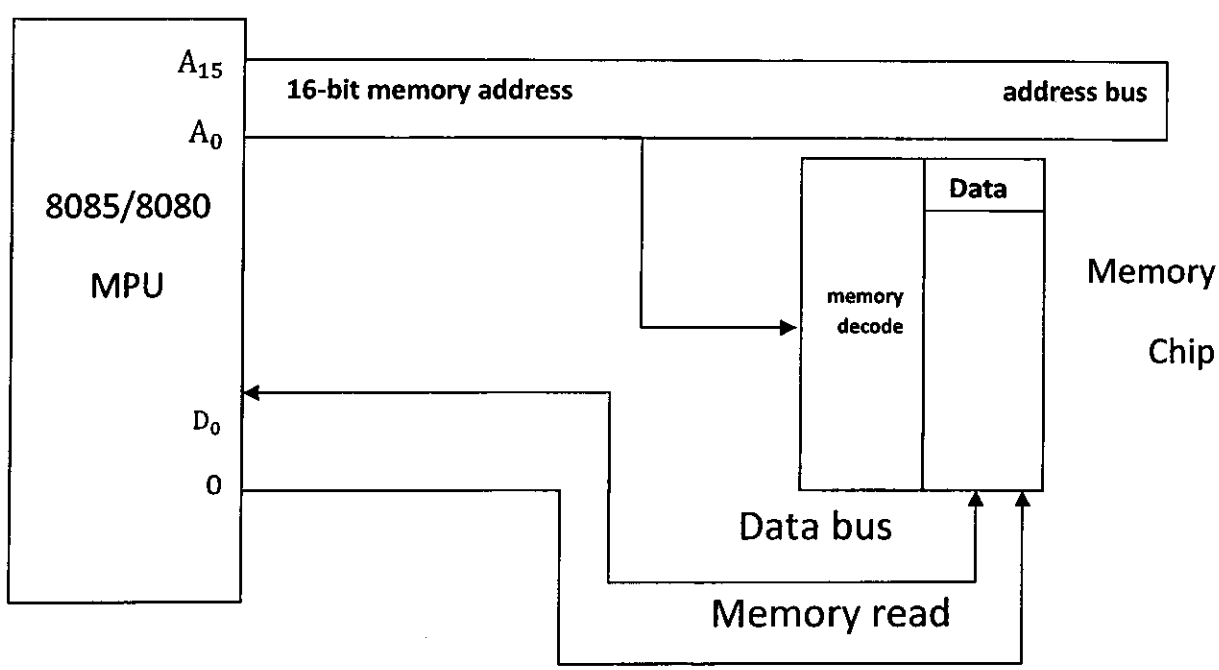
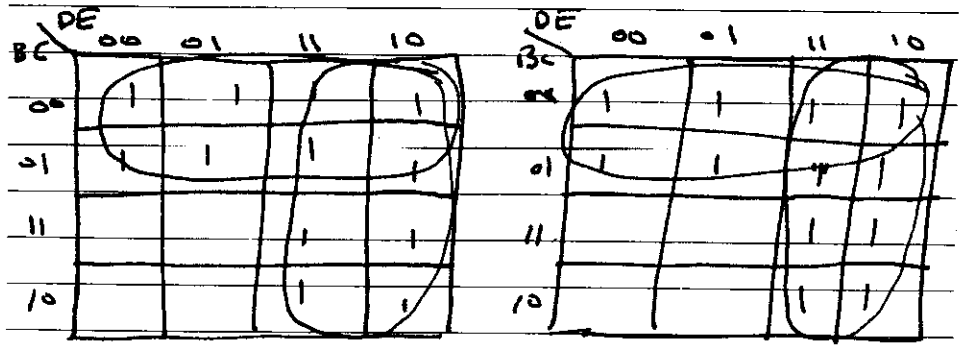


Figure (2). Memory read operation

Q3A



Ans: $F = D + \overline{B}$

Q3B **cycle stealing DMA**:-in this technique , the DMA controller transfers a byte of data between the memory and peripheral device by stealing a clock cycle of the microprocessor . the DMA controller will complete the transfer by passing the microprocessor and generating proper signals to complete the transfer. Since the microprocessor is operated by an external clock, it is quite simple to stop the microprocessor momentarily.

This is accomplished by not providing the clock signal to the microprocessor. An INHIBIT signal is used for this purpose, which is normally HIGH and is logically AND with the system clock to generate the microprocessor clock, as shown in Fig(10-2).

The DMA controller stops the microprocessor by lowering the INHIBIT signal to LOW. A timing diagram is shown in Fig (10-3). The DMA controller then takes over the control of the microprocessor system bus for the time that microprocessor is stopped. Using cycle stealing, data is transferred 1 byte at a time.
The DMA controller requests the microprocessor for each byte to be transferred.

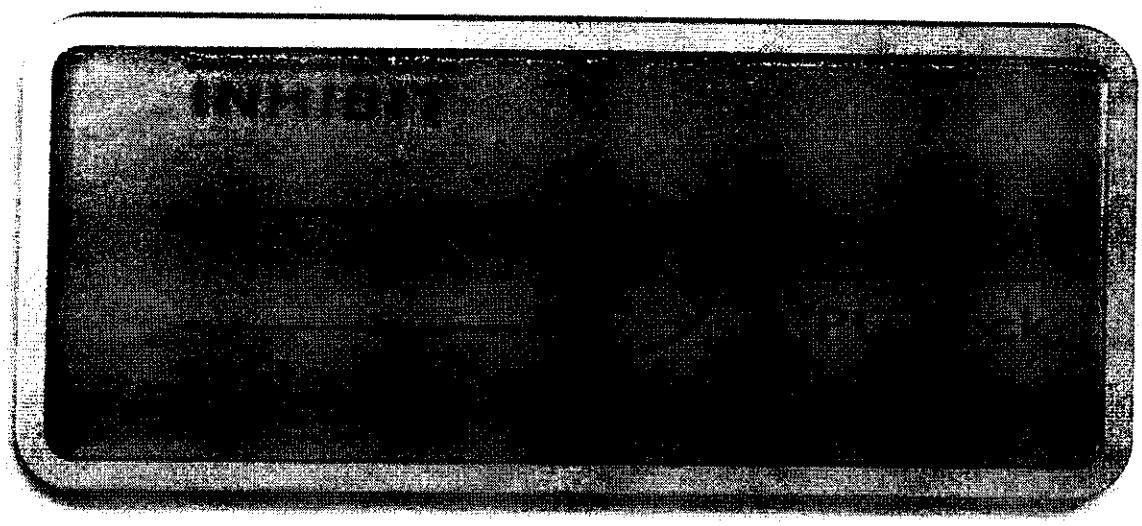


Fig (10-3):- cycle stealing DMA

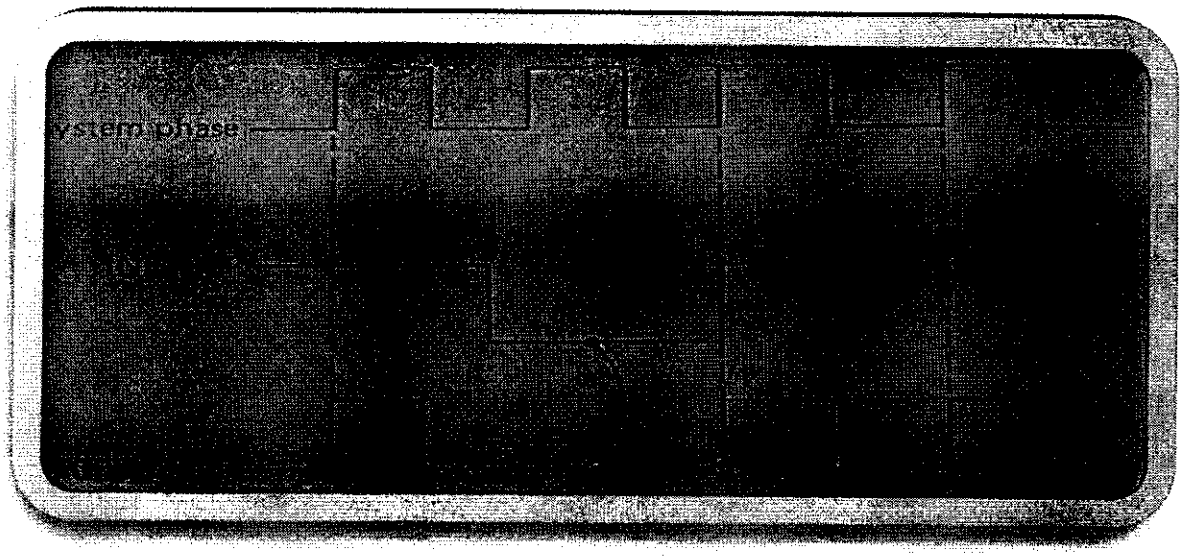


Fig (10-4) cycle stealing DMA timing diagram

Q4A

$D_0 = \bar{B}C$

$D_1 = \bar{B}D$

$D_2 = \bar{B}\bar{D}$

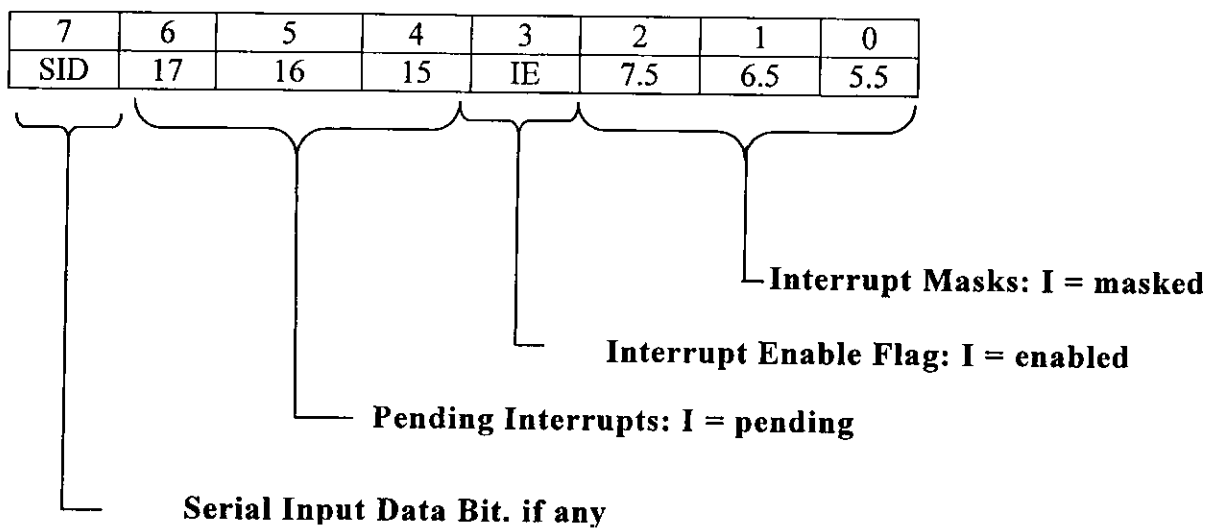
$D_3 = \bar{B}\bar{C}$

Q4B

Pending Interrupts

Because there are several interrupt lines, when one interrupt request is being served, other interrupt requests may occur and remain pending. The 8085 has an additional instruction called RIM (Read Interrupt Mask) to sense these pending interrupts.

RIM instruction loads the accumulator with the following information:



1- Trap

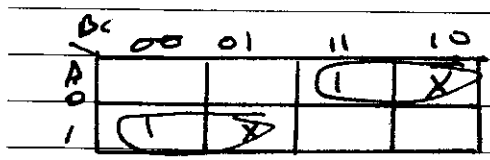
2- RST 7.5

3- RST 6.5

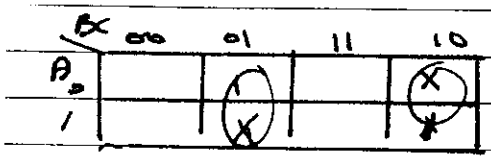
4 - RST 5.5

Q5A

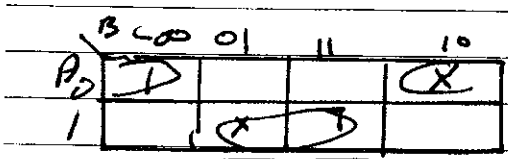
Dec	A	B	C	T_A	T_B	T_C
0	0	0	0	0	0	1
1	0	0	1	0	1	0
3	0	1	1	1	0	0
7	1	1	1	0	0	1
6	1	1	0	0	1	0
4	1	0	0	1	0	0



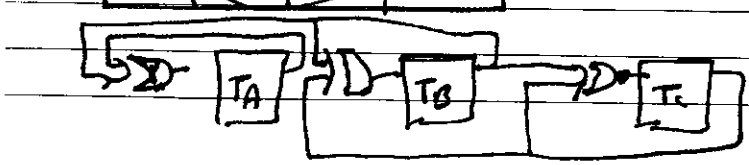
$T_A = A \oplus B$



$T_B = B \oplus C$



$T_C = \overline{B \oplus C}$



```
QSB
    LXI H, A0F9H
    MVI B, 64H
    MNIA, 00
**  MOV A,M
    CMP M
    JP *
    MOV M,A
*   INX H
    DCR B
    JNZ **
    RST1
```

Q26A

$\omega = AB + A\bar{C}\bar{D}$

$X = \bar{B}C + B\bar{C} + B\bar{C}\bar{D}$

$y = C\bar{D} + \bar{C}D$

$z = \bar{D}$

for A, B, C, D as input

and ω, X, y, z as output

$d = \Sigma\, 1, 2, 3, 12, 13, 14$

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Q6 B