حلول نموذج اسئلة - عوض/ رقم -١-

Ministry of Higher Education & Scientific Research
University of Technology
Department of Communication Engineering

DEPARTMENT OF COMMUNICATION ENGINEERING UNIVERSITY OF TECHNOLOGY

قسم هندسة الاتصالات
الجامعة التكنولوجية

Final Examination 2016-2017

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Divisions: All Divisions — *Time: 3 Hours*

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Examiner: Dr. Ali O. Abid Noor — *Number of pages: 1*

Attempt <u>Four</u> questions only

Q1.

Sol.

(a) First, we have to calculate the cutoff frequencies of the highpass and the lowpass filters connected in cascade to produce the required BPF. Each of these filters is a one stage 2-plole filter. We start by dividing the bandwidth value by 2:

$\frac{BW}{2} = \frac{3.48}{2} = 1.92kHz$,

For the HPF;

$f_{c1} = f_0 - 1.92 = 4.95 - 1.92 = 3.03kHz$

And for the LPF;

$f_{c2} = f_0 + 1.92 = 4.95 + 1.92 = 6.87kHz$

Now, we calculate the components values for both filters, starting with the HPF;

In general; $f_c = \frac{1}{2\pi RC}$; for the HPF; $3.03\times10^3 = \frac{1}{2\pi(1\times10^3)C_1}$, $\therefore\ C_1 = C_2 = 0.052\mu F$

For the LPF; $6.87\times10^3 = \frac{1}{2\pi(1\times10^3)C_3}$, $\therefore C_3 = C_4 = 0.032\mu F$

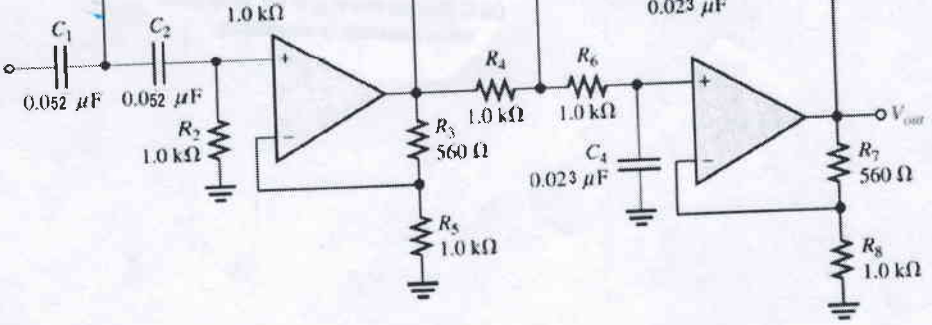
$R_1 = R_2 = R_5 = 1k\Omega$,

For Butterworth response, we treat each filter as a 2-pole one stage filter; therefore, we use the feedback ratio of 0.586 for both filters, hence

$R_3 = 1k\Omega\times0.586 = 586k\Omega$

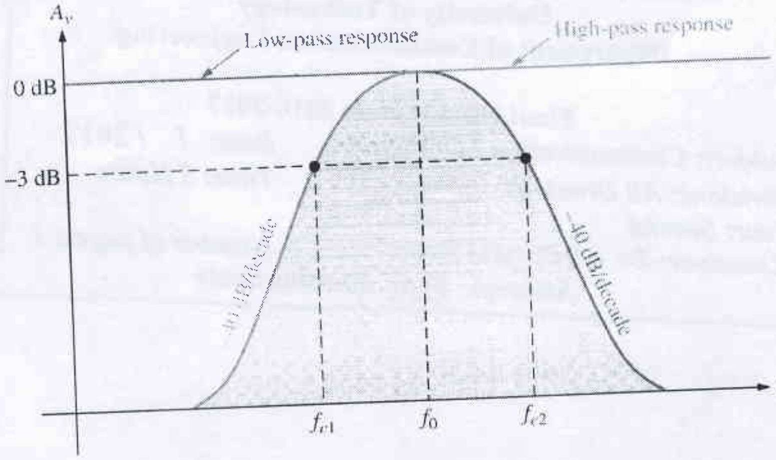
$R_7 = 1k\Omega\times0.586 = 586k\Omega$

An approximate solution with practical component values is shown in the figure below.



(b)

The frequency response of the filter is shown in the figure below, the roll-off of each side is -40 dB/ decade.



Q2.

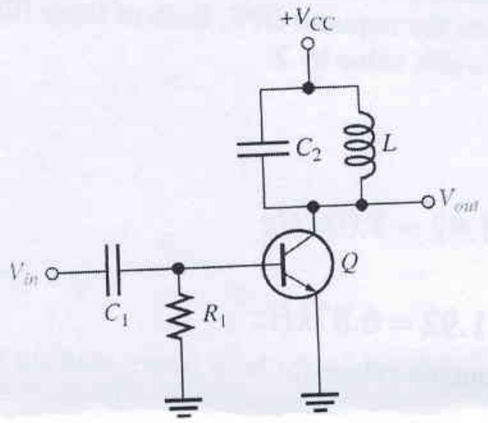
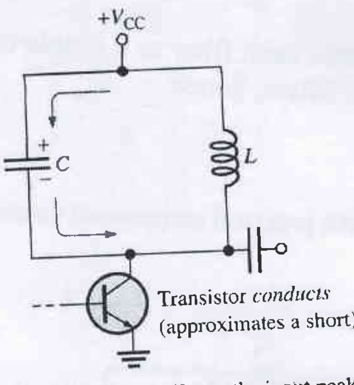
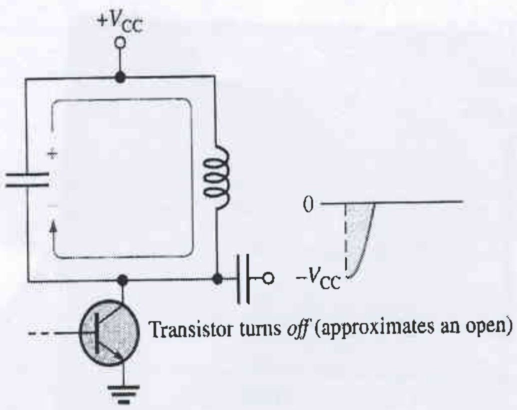


Figure Q2.

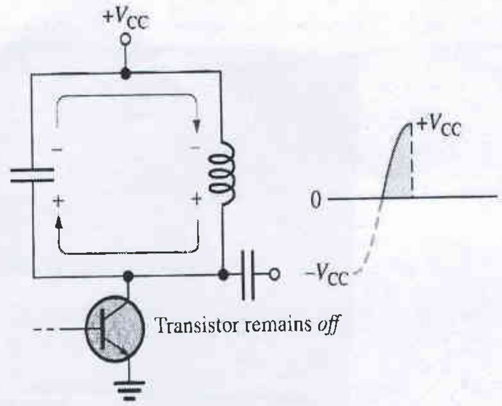
(a)



(a) C charges to $+V_{CC}$ at the input peak when transistor is conducting.



(b) C discharges to 0 volts.



(c) L recharges C in opposite direction.

(b)

$$f_r = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{(10\text{ mH})(0.001\,\mu\text{F})}} = \mathbf{50.3\ kHz}$$

(c)

$$V_{out(pp)} = 2V_{CC} = 2(12\text{ V}) = \mathbf{24\ V}$$

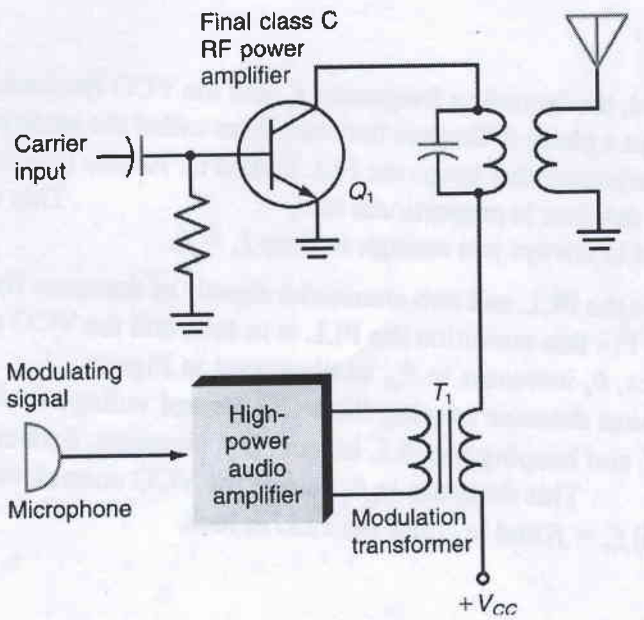
$$P_{out} = \frac{0.5V_{CC}^2}{R_c} = \frac{0.5(15\text{ V})^2}{50\ \Omega} = 2.25\text{ W}$$

$$P_{D(avg)} = \left(\frac{t_{on}}{T}\right)V_{CE(sat)}I_{C(sat)} = (0.1)(0.18\text{ V})(25\text{ mA}) = 0.45\text{ mW}$$

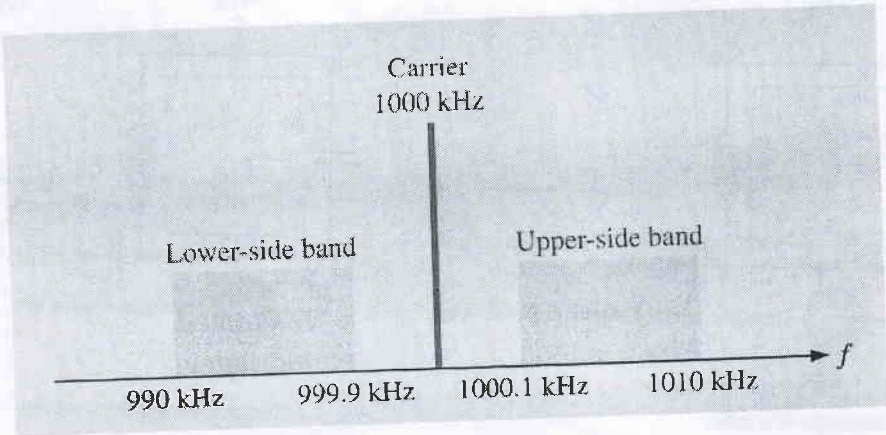
$$\eta = \frac{P_{out}}{P_{out} + P_{D(avg)}} = \frac{2.25\text{ W}}{2.25\text{ W} + 0.45\text{ mW}} = \mathbf{0.9998}$$

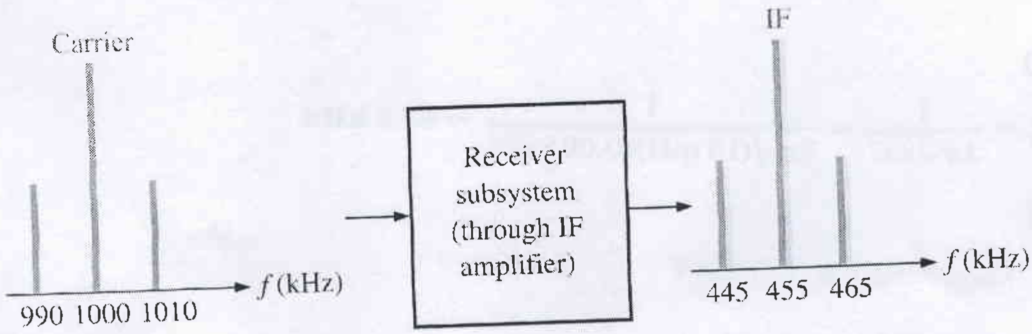
Q3.

Sol. **(a)**

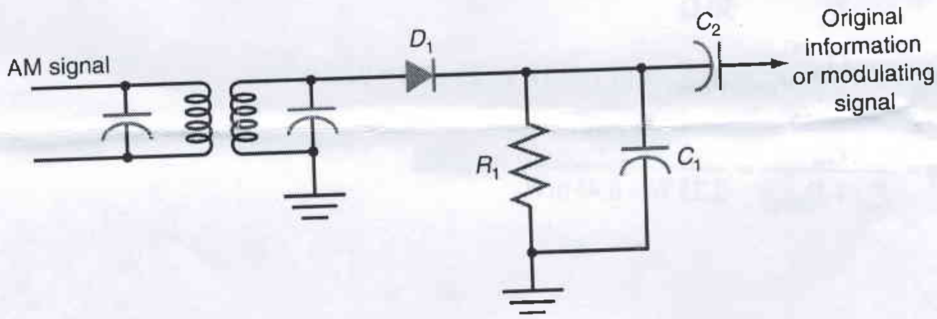


(b)





(c)



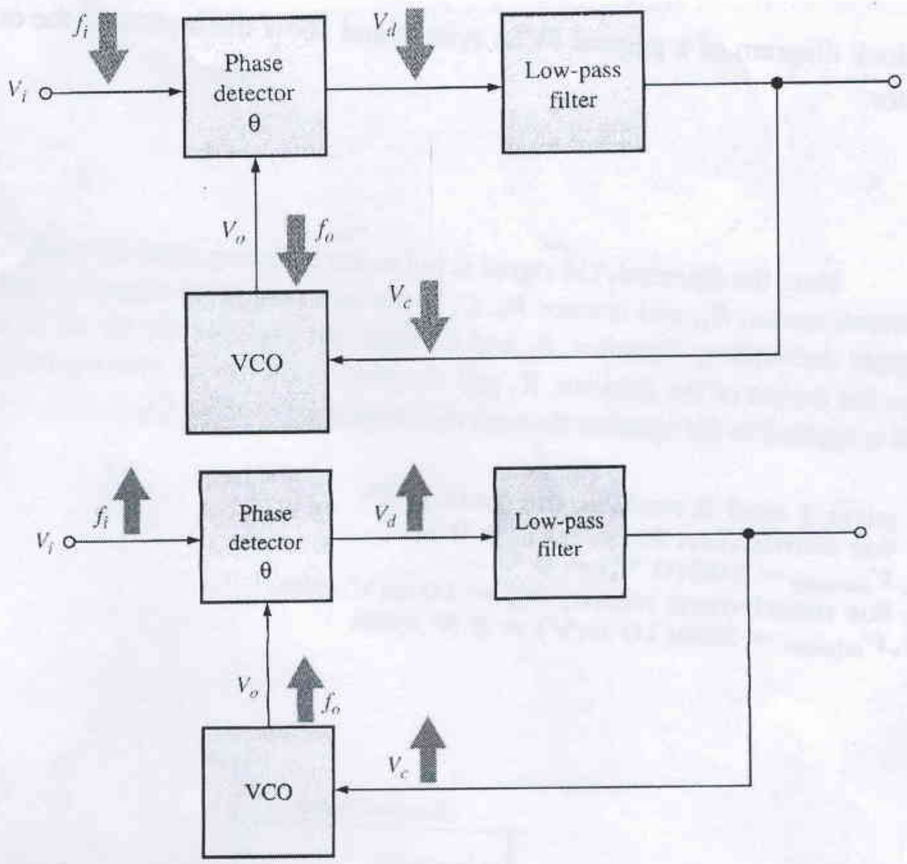
Q4.

Sol.

(a)

When the PLL is locked, the incoming frequency, f_i, and the VCO frequency, f_o, are equal. However, there is always a phase difference between them called the *static phase error.* The phase error, θ_e, is the parameter that keeps the PLL locked in. As you have seen, the filtered voltage from the phase detector is proportional to θ_e . This voltage controls the VCO frequency and is always just enough to keep $f_o = f_i$.

Figure shows the PLL and two sinusoidal signals of the same frequency but with a phase difference, θ_e. For this condition the PLL is in lock and the VCO control voltage is constant. If f_i decreases, θ_e increases to θ_{e1} as illustrated in Figure This increase in θ_e is sensed by the phase detector causing the VCO control voltage to decrease, thus decreasing f_o until $f_o = f_i$ and keeping the PLL in lock. If f_i increases, θ_e decreases to θ_{e1} as illustrated in Figure . This decrease in θ_e causes the VCO control voltage to increase, thus increasing f_o until $f_o = f_i$ and keeping the PLL in lock.



(b)

The free-running frequency:

$$f_o = \frac{1.2}{4R_1C_1} = \frac{1.2}{4(3.9\,\text{k}\Omega)(330\,\text{pF})} = \mathbf{233\ kHz}$$

The lock range:

$$f_{lock} = \pm\frac{8f_o}{V_{CC}} = \pm\frac{8(233\,\text{kHz})}{18\,\text{V}} = \pm\frac{1.864\,\text{MHz}}{18\,\text{V}} = \mathbf{\pm 104\ kHz}$$

The capture range:

$$f_{cap} = \pm\frac{1}{2\pi}\sqrt{\left(\frac{2\pi f_{lock}}{3600\times C_2}\right)}$$

$$= \pm\frac{1}{2\pi}\sqrt{\left(\frac{2\pi(103.6\,\text{kHz})}{3600\times 0.22\,\mu\text{F}}\right)} = \pm\frac{1}{2\pi}\sqrt{\left(\frac{650.9\,\text{kHz}}{792\,\mu\text{F}}\right)} = \mathbf{\pm 4.56\ kHz}$$

The capture range can be increased by decreasing C_2.

Q5. (a) Discuss the function of the components of the audio amplifier shown in Figure Q5 and determine the maximum and the minimum output voltages for the audio power amplifier shown in figure Q5 if the input voltage from the detector is 10 mV rms. Given the gain of the LM386 is 200

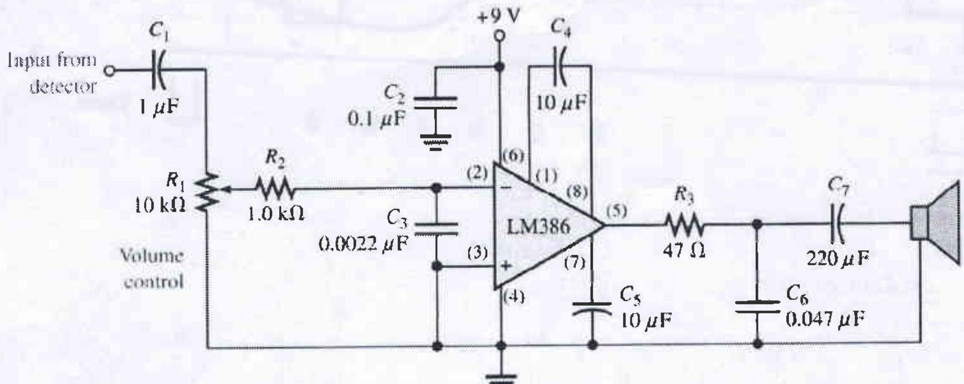


Figure Q5. The LM386 audio amplifier circuit.

(b) Draw a block diagram of a general PCM system and show the input and the output of a delta modulator.

Sol.

(a)

Here the detected AM signal is fed to the inverting input through the volume control potentiometer, R_1, and resistor R_2. C_1 is the input coupling capacitor and C_2 is the power supply decoupling capacitor. R_2 and C_3 filter out any residual RF or IF signal that may be on the output of the detector. R_3 and C_6 provide additional filtering before the audio signal is applied to the speaker through the coupling capacitor C_7.

C_4 between pins 1 and 8 makes the gain 200.
With R_1 set for minimum input, $V_{in} = 0$ V.
$V_{out(min)} = A_v V_{in(min)} = 200(0\ \text{V}) = \mathbf{0\ V}$
With R_1 set for maximum input, $V_{in} = 10$ mV rms.
$V_{out(max)} = A_v V_{in(max)} = 200(10\ \text{mV}) = \mathbf{2\ V\ rms}$

(b)