Design and Simulation of Sigma-Delta Fractional-N Frequency Synthesizer for WiMAX

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Abstract
This paper presents a design and simulation of proposed frequency synthesizer which can be used for WiMAX. Design parameters for the proposed fractional-N PLL synthesizer for WiMAX system are either selected from WiMAX standards or according to results of analysis for each unit of the proposed system. Different techniques for phase noise reduction are discussed. Sigma-delta fractional-N technique is chosen for WiMAX system, since low settling time, spurious level and phase noise can be obtained by using this technique. The simulation result shows the system is stable, since the phase margin is greater than 45 degree. The settling time, spurious level and phase noise obtained with this synthesizer are 5.9μs, -90dBc/Hz, and -100dBc/Hz respectively. CppSim program (C++ simulator language) and Matlab (V.7) are used for simulation of $\Sigma\Delta$ fractional-N PLL synthesizer.

Keywords: WiMAX, Frequency synthesizer, PLL, Spur-suppression technique, Fractional-N frequency synthesizer.

تصميم و محاكاة مركب التردد من نوع(Sigma-Delta Fractional-N) لمنظومة WiMAX

WiMAX.

WiMAX

(Sigma-Delta   .   .

.   WiMAX   Fractional-N)

5.9μs

CppSim(C++ simulator language)   .   -100 dBc/Hz -90 dBc/Hz

.(sigma-delta ($\Sigma\Delta$) fractional-N)   Matlab (V.7)

Introduction

WiMAX is a wireless metro-politan area network (WMAN) technology that provides interoperable broadband wireless connectivity to fixed, portable, nomadic and mobile users [1]. It provides up to 50 Km of service area under line of sight (LOS) condition and up to 8 Km under non line of sight (NLOS), and provides total data rates up to 75 Mbps to support simultaneously hundreds of businesses and homes with a single base station. WiMAX improves the last-mile delivery aspects of multipath interference and delay spread [2,3]. Multi-path interference and delay spread improve performance in situations where there is no direct line-of-sight (NLOS) path between the base station and the user station. However, common to almost all of these standards is that the data

to be transferred is somehow modulated on a radio frequency (RF) carrier, and the modulated signal is then transmitted over the air. The received signal is demodulated at the receiving end, an accurate RF carrier signal must be generated. Therefore, a radio frequency synthesizer is required in transmitter and receiver for all wireless communication systems. Most important part to all wireless systems is frequency synthesizer (FS).

A frequency synthesizer (FS) is a device that generates one or many frequencies from one or a few frequency sources [2]. Practically all communication systems use local oscillator (LO) based on frequency synthesis [2].

The frequency synthesizer is used in the receiver or transmitter, as a part of a larger radio communication system. The receiver must be sensitive, selective, and able to detect even a weak signal among many other, possibly stronger signals. Therefore, a good receiver must have an accurate local oscillator frequency, and low-noise components. However, a transmitter must produce a signal that has enough power, very accurate frequency and clean enough spectrum. Most synthesizers in radio frequency (RF) applications are based on the phase-locked loop (PLL) principle, as shown in Figure (1). A basic PLL is made up of four building blocks: Phase-frequency detector (PFD) with charge pump (CP), low pass filter (LPF), VCO, and a divider. An output signal of frequency f_{out} is generated, and f_{out} is divided by N. The output of the divider is a signal with low frequency (f_{out}/N), which is sent to the PFD. At the PFD, the phase and frequency of the signal are compared

with an external signal of frequency (f_{Ref}), which is generated using a crystal oscillator. The output signal of the PFD and CP is then low pass filtered, and the filtered signal is sent to the VCO input to control the frequency of the output signal [3]. The disadvantage of this technique is the output frequency is equal to multiple of the reference frequency ($f_{out} = N \times f_{Ref}$), where N, the loop frequency divide ratio, is an integer. The frequency resolution of the integer-N frequency synthesizer is equal to the reference frequency [3]. The conventional integer-N PLL with low reference frequency has several disadvantages. First, the lock time is long due to its narrow loop-bandwidth. Second, the reference spur and its harmonics are located at low offset frequencies. Third, the large divide ratio (N) increases the in-band phase noise associated with the reference signal. Finally, with a small loop-bandwidth, the phase noise of the VCO will not be sufficiently suppressed at low offset frequencies [3]. The most well accepted solution to these problems [3] is the fractional-N PLL that is discussed in next section.

2.   Fractional-N   Frequency Synthesizer

In integer-N synthesizer, the minimum resolution is equal to the reference frequency. In order to get a finer resolution, a fractional-N technique is used to achieve frequency resolution finer [5,6] than the reference frequency, as shown in Figure (2a). The output frequency f_{out} can be varied in fractional increments of reference frequency. The fractional part of divider is

implemented using phase accumulator [5].

The main source of problems in fractional-N synthesizers is when an overflow occurs in the accumulator, the divider ($\div N / N + 1$) is divided by N+1 for one period, corresponding to a 2π decrease in the phase error at the phase detector input, as shown in Figure (2b). The resulting phase error causes spurious tones at the output frequency [5].

2.1 Spur-Suppression Techniques

The classical approach to fractional-N synthesizer design [5,7] employs dithering and phase interpolation (PI), as shown in Figure (3). An accumulator carry-out signal is used to dither the control input to a multi modulus divider. The DAC is used to convert the instantaneous phase error, which is proportional to the residue of the accumulator, into an equivalent amount of charge-pump current to compensate the phase error [7]. The main limitations with this architecture center around the achievement of a good matching between the DAC output and phase-error signal. This matching is difficult to obtain because the two signals are processed by separate circuits whose outputs are summed. Any gain mismatch between PFD error and DAC output will lead to spurious tones at PLL output.

The second technique uses a sigma-delta modulator. This technique is based on oversampling and noise shaping to reduce the phase noise [5,6,8]. The quantization noise-bandwidth tradeoff associated with $\Sigma\Delta$ fractional-N synthesis can be removed if quantization noise can be reduced. The combination of PFD and DAC in one single element is used to overcome non-idealities between them, as shown in Figure (4).

The key advantage of this method is that the circuitry that injects quantization noise into the loop (the PFD and charge-pump) is combined with the cancellation signal by DAC to create an inherent gain match between the two signals. The resulting mismatch compensated PFD/DAC synthesizer is capable of dramatically reducing quantization induced phase noise [9,10].

3. System Description

The PFD/DAC block diagram [10,11] is depicted in Figure (5). A register based delay cell is used to create a delayed divider phase. These signals then pass through a timing mismatch compensation and resynchronization block, which accounts for timing mismatches in the two critical phase information paths.

The two output phases from the timing mismatch compensation and resynchronization block are compared to a reference via two phase detectors that control the charge-pump.

The output of the digital $\Sigma\Delta$ shown in Figure (5) transfers input to the DAC mismatch shaping block which accounts for errors between the unit elements which feed the charge-pump. The output of the DAC mismatch shaping block controls a bank of current source DAC elements sent to the phase detector controlled charge-pump. The output of the charge-pump is sent to the loop-filter.

4. The Description of the Designed Frequency Synthesizer

4.1 Design of Loop Filter

The loop filter schematic shown in Figure (6) consists of two resistors (R_2 and R_3) and three capacitors (C_1, C_2 and C_3). A complete design [12] can be found in appendix A. This filter generates the VCO control voltage according to the current from

the charge pump. However, additional RC low pass filter (R_3 and C_3) can optionally be added in order to reduce the reference spur level, as shown in Figure (6).

4.2 Design of Sigma-Delta Modulator

A third order MASH $\Sigma\Delta$ modulator is chosen as the modulus controller to adjust the frequency of the synthesizer. The design parameters of $\Sigma\Delta$ modulator are shown in Table (1).

4.3 Design of PFD, Charge Pump and S/H

The tri-state-based on PFD consists of two D flip-flops with additional logic to reset the latches [5]. Tri-state PFD is therefore said to be Phase and frequency sensitive. When the rising edge of the $f_{\mathrm{Re}f}$ leads f_{Div}, the PFD output up-signal is high and the PFD output down-signal is low. Thus, the loop filter output voltage increases and so do the VCO output frequency and phase. When the rising edge of the $f_{\mathrm{Re}f}$ lags f_{Div}, the PFD output down-signal is high and the PFD output up- signal is low. Thus, the loop filter output voltage decreases and so do the VCO output frequency and phase. For a frequency synthesizer, a tri-state phase-frequency detector (PFD) is used always. The design parameters of PFD, charge pump, and S/H circuit are shown in Table (2).

4.4 Design of VCO

There are several ways to design a VCO and the most popular structure is the LC VCO [13]. The LC VCO uses a varactor and inductor to produce an oscillating signal. The tuning range of the LC VCO is very small with low phase noise performance. The design specification of VCO is shown in Table (3).

5. Simulation Results

5.1 DAC Quantization Noise Simulation

Figure (7) shows the simulation results of $\Sigma\Delta$ MASH modulator. The quantization noise of first $\Sigma\Delta$ modulator is perfectly cancelled by using the second order digital $\Sigma\Delta$ modulator. However, the third order $\Sigma\Delta$ MASH is suggested to eliminate quantization noise. Simulation results show an improvement of 149 dB in signal-to-noise ratio (SNR) at the output of the third order $\Sigma\Delta$ modulator (which is used to control DAC elements) instead of 109.3 dB for the second order $\Sigma\Delta$ modulator, as shown in figure (7).

5.2 Phase Noise Simulation

Figure (8) presents the result of simulation. In this simulation, the reference spur magnitude is -90dBc/Hz. A sample-and-hold (S/H) is used to eliminate shape mismatch related spurs as shown in simulation results in Figure (9) (if compared with the simulation results shown in Figure (8)).

Figure (10) shows the final simulation result of the PFD/DAC synthesizer. The broadband noise is greatly reduced achieving high levels of fraction spur rejection at the output spectrum of PLL. The overall phase noise performance of the synthesizer, as shown in Figure (10) is good. It meets the equivalent of the WiMAX requirements at 2.566GHz, and meets the reduced spurious goal. Also these results show the effectiveness of the proposed system in reduction of the phase noise and spurs. Table (4) shows the final phase noise results of the PFD/DAC PLL synthesizer.

5.3 Stability of PFD/DAC PLL and Settling Time Simulation Results

Figure (11) shows Matlab simulation results of the open-loop frequency response. The crossover frequency is

2.36Mrad/s and the phase margin is 56.3°. Since the phase margin is greater than 45 degrees, the system is stable. The step response is performed to check the settling of the system. The settling time is defined as the time required for the response to decrease to end state with in specified present of it final value. A frequently used 5% [14]. The step response plotted in Figure (12). The settling time is 5.9μsec.

6. Conclusions

1. The ΣΔ fractional-N PLL is designed to generate 2.566 GHz according to IEEE 802.16e WiMAX specification (2.3GHz-2.7GHz), with following main characteristics:

- Short settling time 5.9μs as shown in figure (12)
- The spurious output is -90 dBc/Hz
- Phase noise is no less than -95 dBc/Hz in band
- Bandwidth of system is 1MHz

2. The C++ language, is used in the simulation of the computing system behavior for any blocks of the synthesizer due to its flexibility and high speed of execution.

3. ΣΔ fractional-N PLL technique is selected to WiMAX system since it has the following advantages:

- Large loop bandwidth
- Short settling time
- Step size smaller than an integer-N PLL

4. The quantization noise of second ΣΔ modulator is perfectly cancelled by using third order digital ΣΔ modulator (SNR= 149 dB).

7. References

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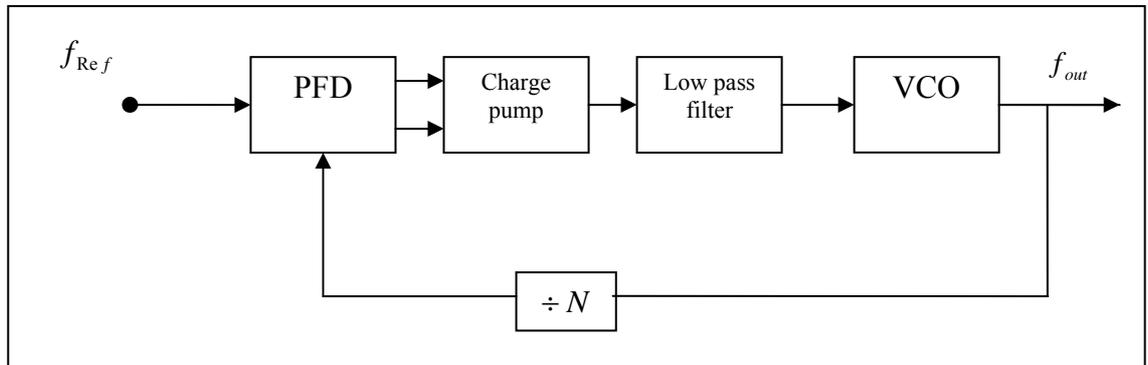
Figure (1): The block diagram of phase-locked loop.
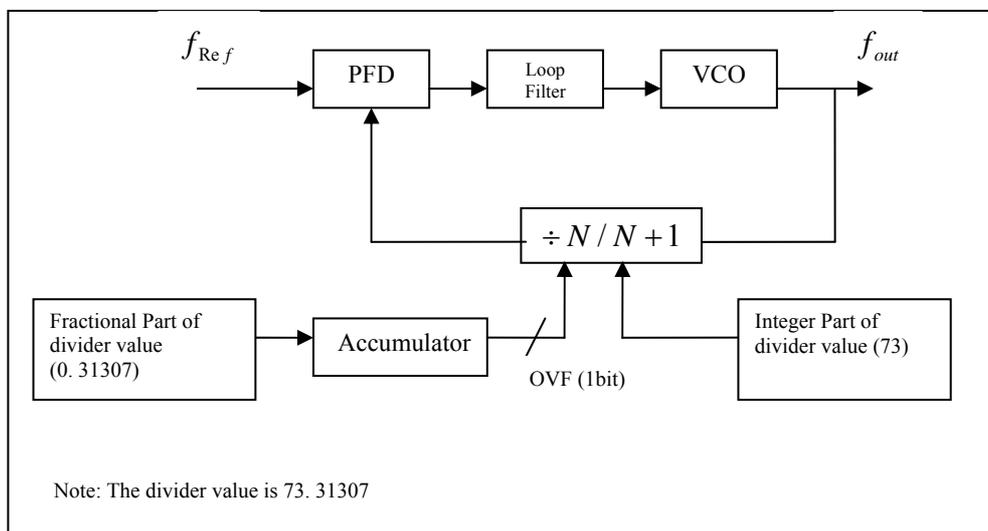
(a)
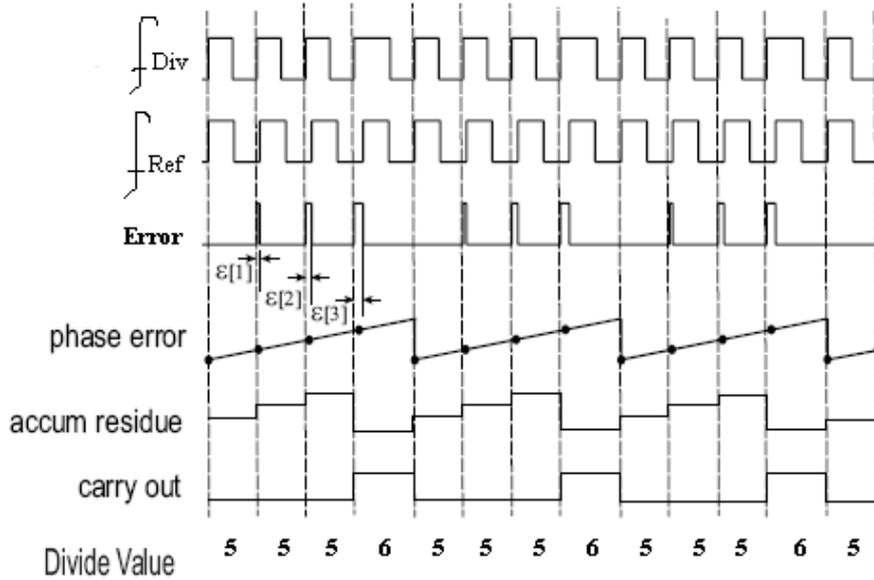
(b)

Figure (2): (a) Classical fractional-N synthesizer
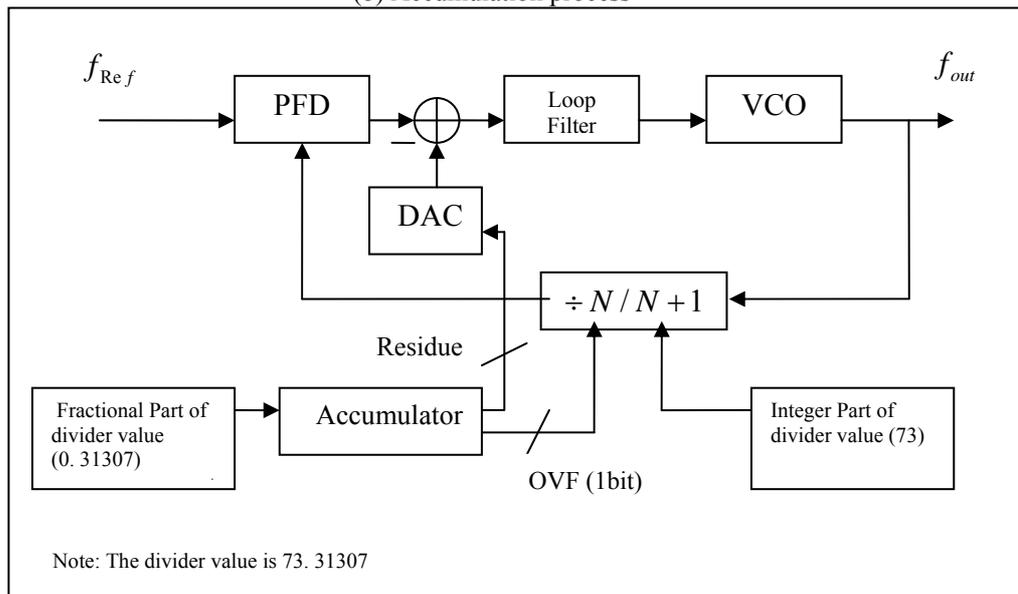(b) Accumulation process
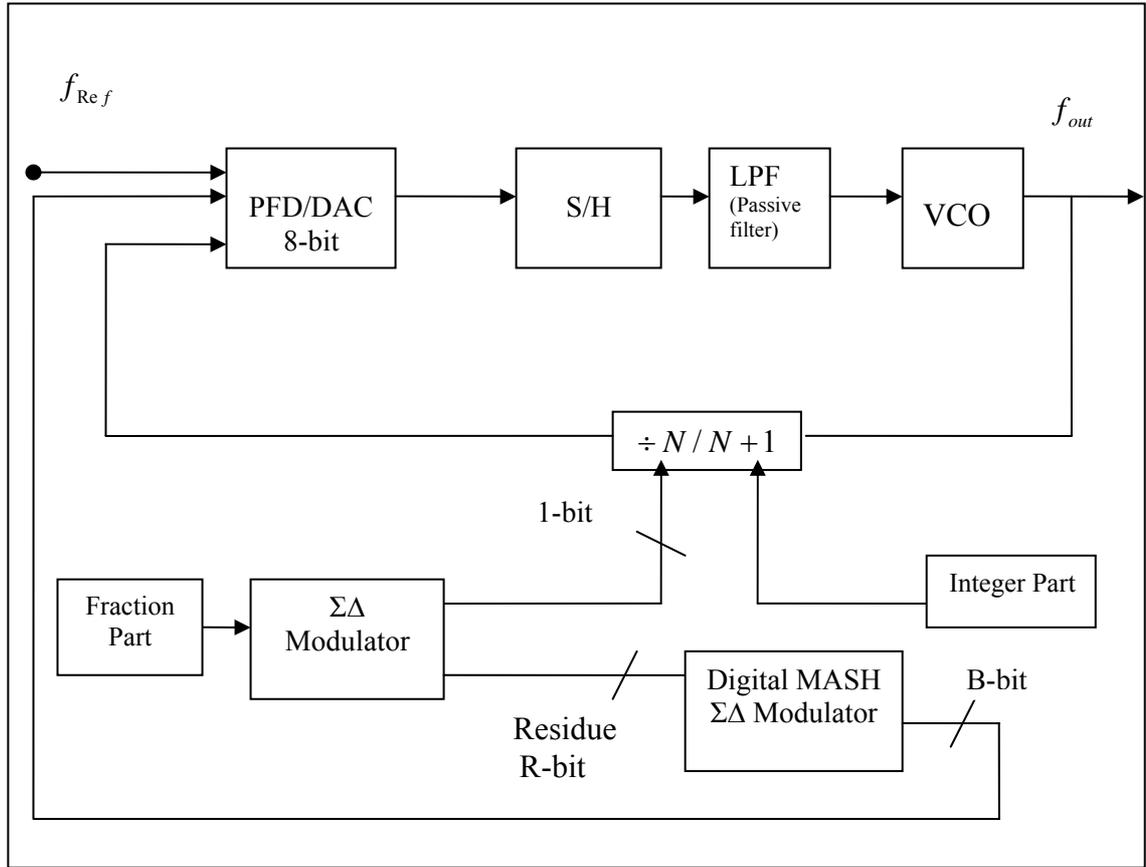

Figure (3): Phase interpolation technique.

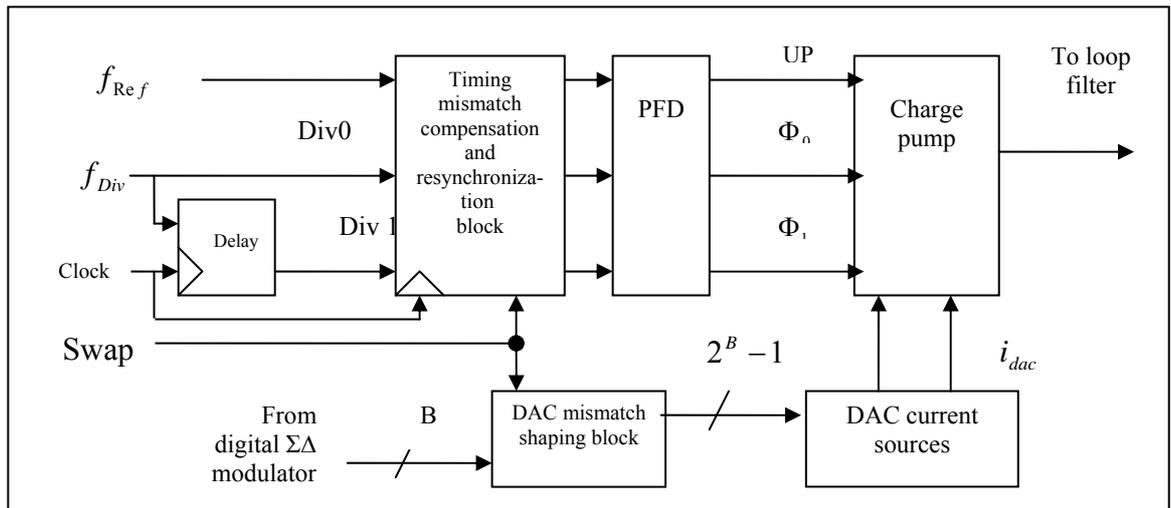Figure (4): Sigma-delta technique with hybrid PFD/DAC structure.

Figure (5): PFD/DAC block diagram.
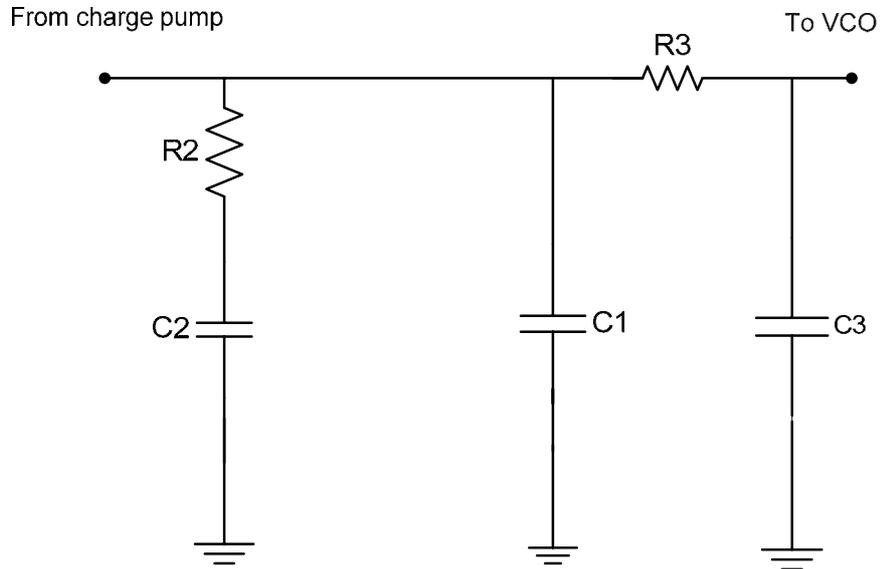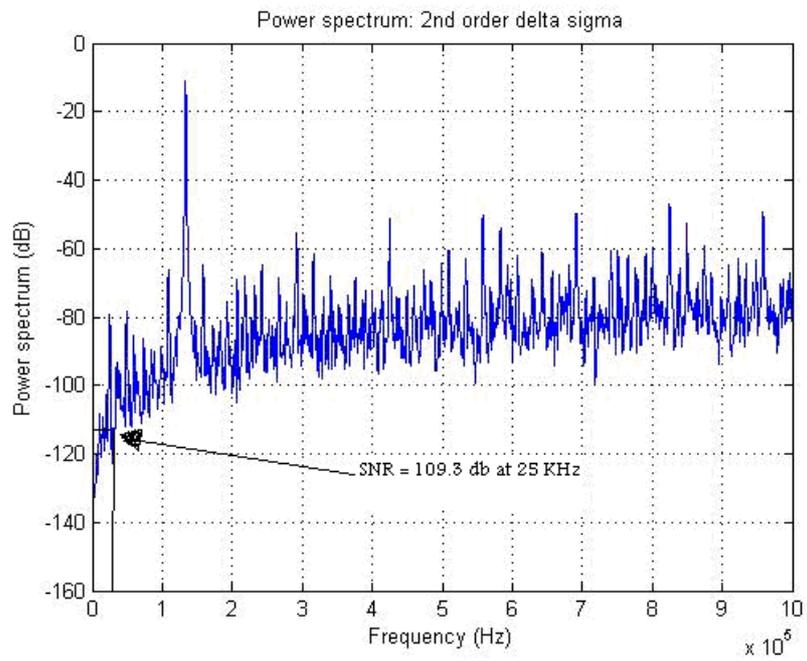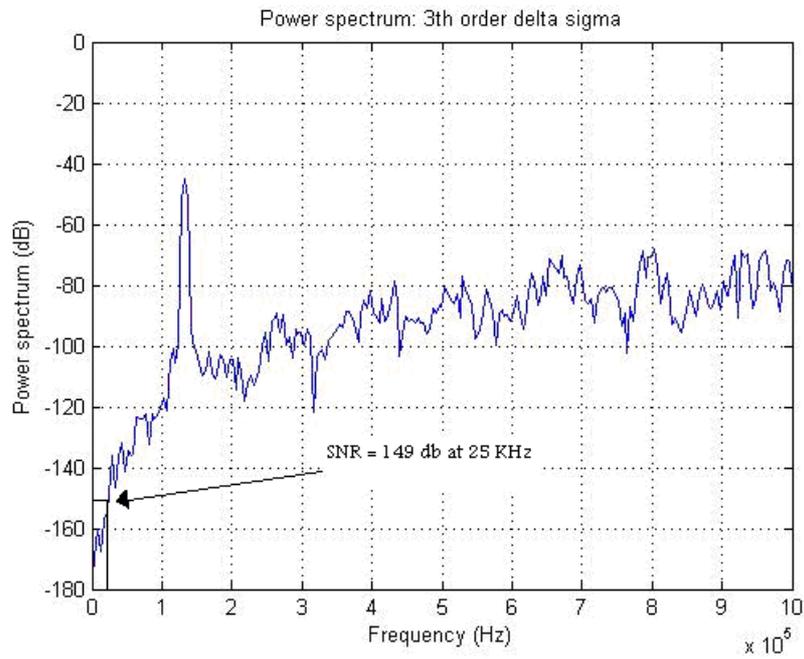
Figure (6): Second order lead-lag loop Filter with added pole.

(a)

(b)

Figure (7): Simulation of ΣΔ MASH quantization noise spectrum.
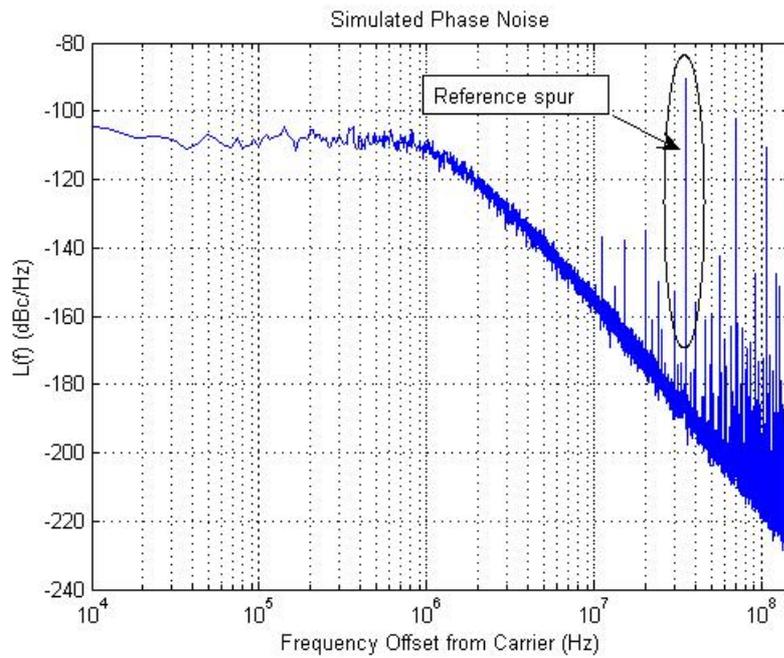(a)   Second order 8-bit ΣΔ MASH (b) Third order 8-bit ΣΔ
MASH

Figure (8): Simulation showing a residual spur at output of 8-bit
PFD/DAC synthesizer due to shape mismatch
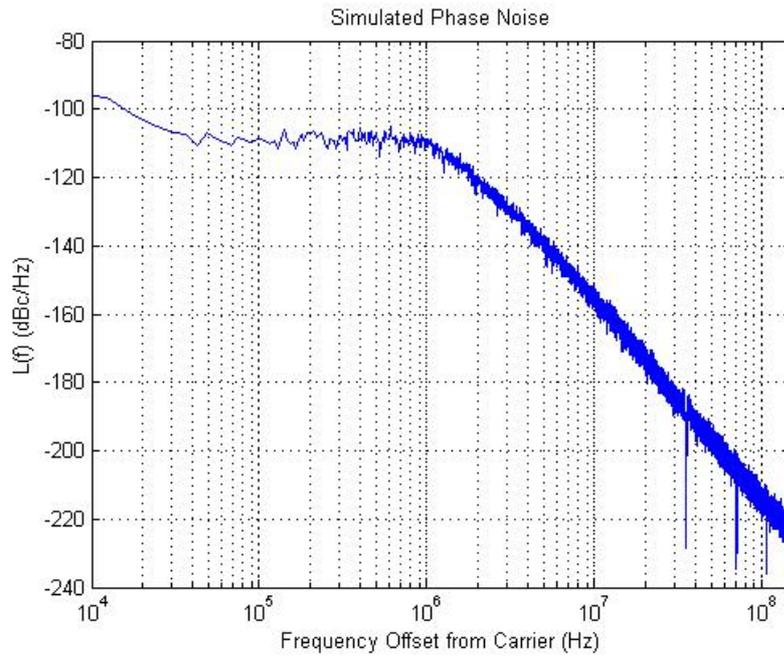with spur level= -90 dBc/Hz.

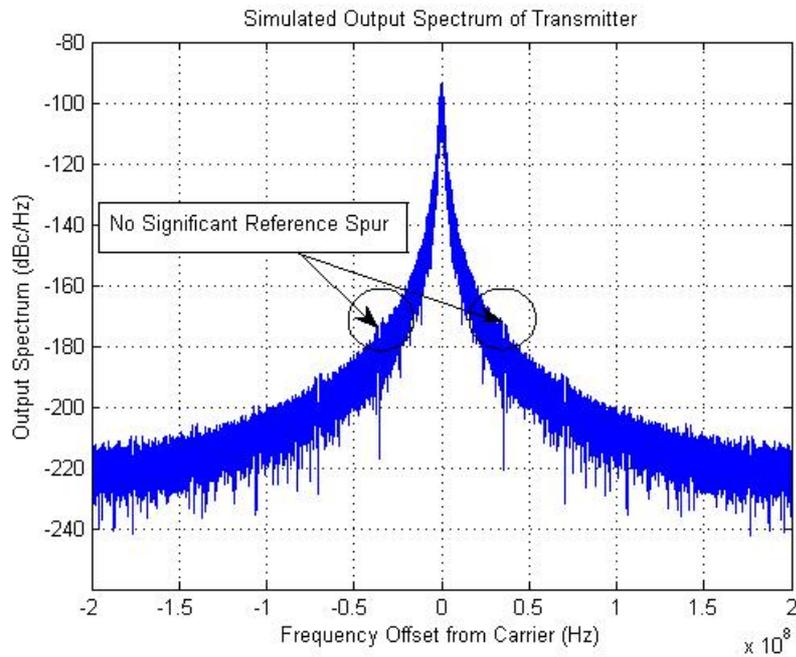Figure (9): Simulation showing a phase noise.

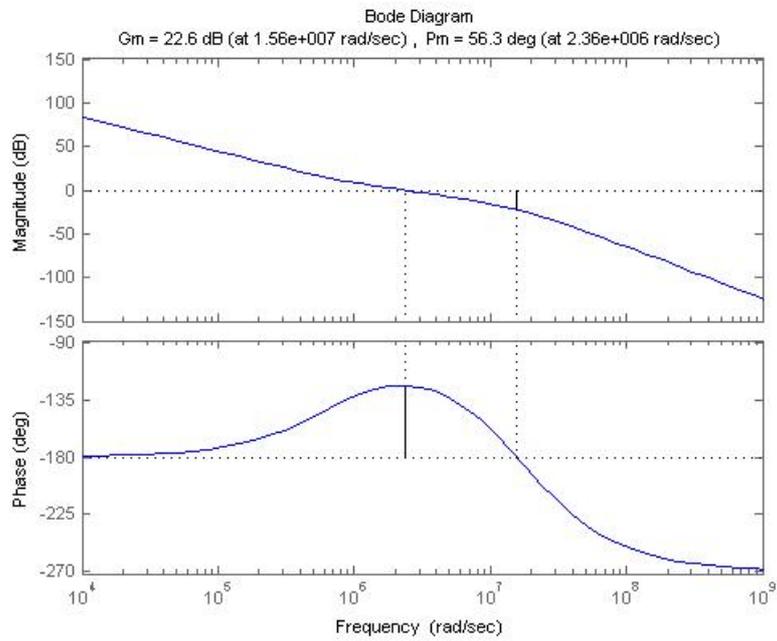Figure (10): Output spectrum of PFD/DAC synthesizer for 2.566GHz.

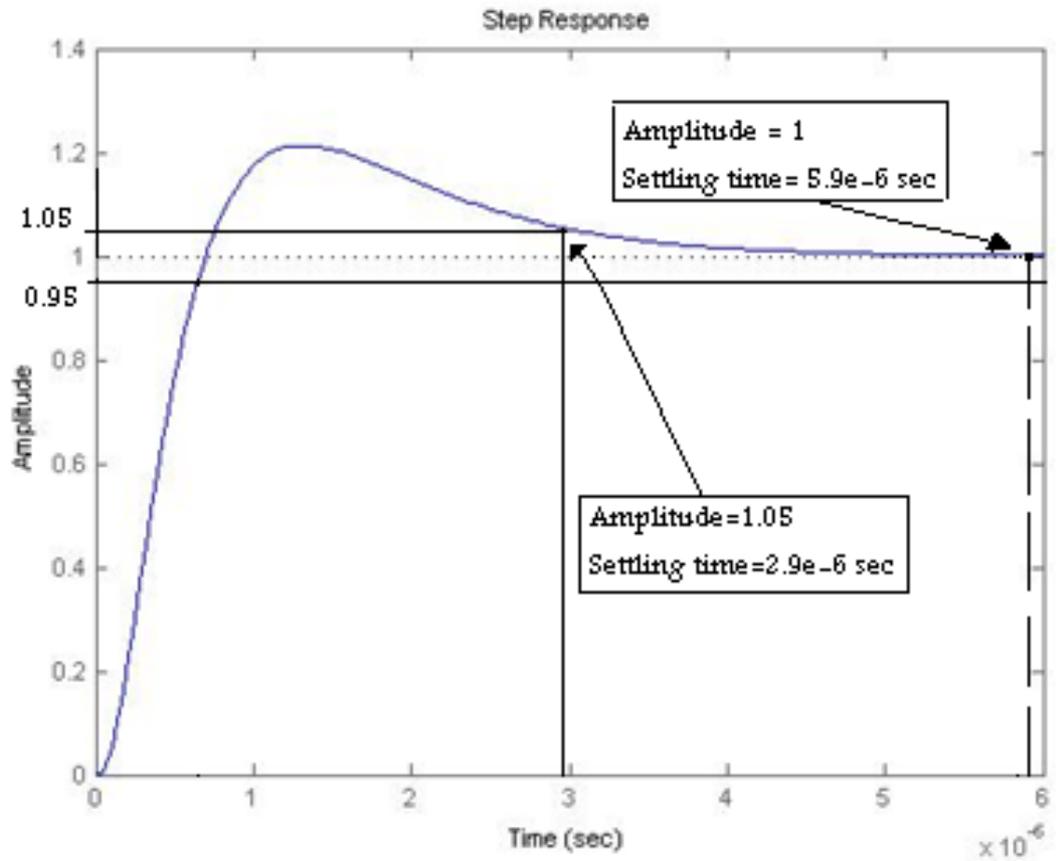Figure (11): Simulation showing open-loop response.

Figure (12): Step response for PFD/DAC PLL synthesizer.

Table (1): Sigma-delta modulator parameters.

Parameter	Value
Input frequency	68KHz
Sampling frequency (f_S)	35e6
Oversampling rate (OSR)	257
SNR	149dB
Decimation rate	10

Table (2): The basic requirements of PFD, charge pump, and S/H circuit.

Parameter	Value
Charge pump Current	5mA
S/H Capacitors	50pF
Delay duration	3ns

Table (3): VCO parameters.

Parameter	Value
VCO topology	LC Tank
VCO sensitivity (K_{vCO})	200 MHz/V

Table (4): Summarizes the simulation results.

Parameter	Proposed system	WiMAX requirement
Output frequency	2.566GHz	2.3GHz-2.7GHz
Loop bandwidth	1MHz	<100KHz
Phase noise	-95 dBc/Hz@10KHz - 110dBc/Hz@100KHz -110dBc/Hz@1Mhz	-58 dBc/Hz@10KHz -71dBc/Hz@100KHz -98dBc/Hz@1Mhz
Reference frequency	35MHz	<30MHz
Charge pump current	5mA	To reduce charge pump noise at the PLL output
Filter (Order/Response)	Third order/ Butterworth	Third order/Butterworth
Divider	73.31307	Integer division between (64-78)
ΣΔ modulator	Third order	Third order
PFD/DAC resolution	8-bit	(It is not defined by WiMAX forum until now)

Appendix A

PLL Design Assistant (PDA) program, calculates the required values of the loop filter pole and zero, to achieve the desired bandwidth and filter response, as shown in table (A.1).

Table (A.1) Loop filter parameters.

Parameters	Value
Loop filter pole (f_p)	2.8 MHz
Loop filter zero (f_Z)	111 KHz
Added filter pole ($f_{addpole}$)	2.4 MHz

These values assume a lead-lag loop filter, as described in section (4.1). The loop filter parameters (C_1, C_2, C_3, R_2, R_3), as shown in figure (6), are derived based on the following equations:

$$\tau_1 = \frac{1}{2\pi.f_p} = \qquad\qquad\qquad 56.69930 \times 10^{-9} \text{ sec}$$

(A.1)

$$\tau_2 = \frac{1}{2\pi.f_z} = \qquad\qquad 1.432537 \times 10^{-6} \qquad\qquad \text{sec}$$

(A.2)

$$\tau_3 = \frac{1}{2\pi.f_{addpole}} = 66.31455 \times 10^{-9} \text{ sec}$$

(A.3)

$$\omega_C = \sqrt{\frac{1}{\tau_2.(\tau_1 + \tau_3)}} = 2.4 \qquad\qquad\qquad \text{Mrad/s}$$

(A.4)

where ω_C is a crossover angular frequency

$$C_1 = \frac{\tau_1}{\tau_2} . \frac{K_{VCO}.K_\phi}{\omega_C^2 \times N} * \left[\frac{1 + \omega_C^2 \times \tau_2^2}{(1 + \omega_C^2 \times \tau_1^2)(1 + \omega_C^2 \tau_3^2)} \right]^{\frac{1}{2}} = 327.8 \qquad \text{pF}$$

(A.5)

$$R_3 = \frac{\tau_3}{C_3} = \qquad\qquad\qquad 2 \qquad\qquad\qquad \text{K}\Omega$$

(A.9)

$$\omega_n = \sqrt{\frac{K_\phi.K_{VCO}}{N.(C_1 + C_2 + C_3)}} = 1.277 \qquad\qquad \text{Mrad/s}$$

(A.10)

$$\zeta = \frac{R_2.C_2}{2} . \sqrt{\frac{K_\phi.K_{VCO}}{N.(C_1 + C_2 + C_3)}} = 0.92$$

(A.11)

Where N is the divider value (73.31307)

$$\omega_d = \omega_n * \sqrt{1 - \zeta^2} = 500 \text{ Krad/s}$$
(A.12)